Top-gate organic field-effect transistors fabricated on paper with high operational stability

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ABSTRACT: We report on top-gate organic field-effect transistors (OFETs) fabricated on specialty paper, PowerCoat™ HD 230 from Arjowiggins Creative Papers coated with a buffer layer composed of a polyvinyl alcohol (PVA) and polyvinylpyrrolidone (PVP) blend. OFETs operate at low voltages and display average carrier mobility values of $1.7 \pm 1.1 \times 10^{-1} \text{ cm}^2/\text{Vs}$, average threshold voltage values of $-1.4 \pm 0.2 \text{ V}$, and average on/off current ratio of 10^5 . OFETs also display excellent operational stability demonstrated by stable 1000 scans of the transfer characteristics and by stable on-currents displaying less than 6% change during a DC bias stress test at $V_{\text{DS}} = V_{\text{GS}} = -10 \text{ V}$ for 1 h. Furthermore, OFETs on paper display a decrease of only 7% in their on-state current during a bending test. The performance of these OFETs on paper is comparable to that displayed by top-gate OFETs with the same geometry fabricated on glass substrates.

1. Introduction

Paper is perhaps the most economical, ecologically-friendly and sustainable material onto which printed electronics can be built upon. Organic field-effect transistors (OFETs) can be fabricated at low-temperatures over large areas and with fabrication methods that are compatible with roll-to-roll processing techniques; widely used in the paper industry. However, fabricating printed electronics on paper is challenging because its fibrillar nature leads to porous films, with a large surface roughness [1], that are not appropriate for the fabrication of the ultrathin layers required for the realization of an OFET. To overcome this problem, two approaches have been proposed in the literature. In the first approach, ionic gate dielectrics (paper-based, ion gels, polymer electrolytes, etc.) have been used for the realization of ion modulated transistors at low operating voltages. This approach has been demonstrated using both metal-oxide [2] as well as organic thin-film transistors [3, 4]. In the second approach, a buffer layer (either the gate dielectric or a separate layer coating the paper) is used to reduce its surface roughness [5-15] and to insulate the device structure from chemical impurities on the surface of the substrate [11].

In the literature, most studies report on bottom-gate OFETs on paper [5-7, 9, 10, 12-15] wherein the gate electrode and gate dielectric planarize the paper's surface on the channel region or, wherein a planarization layer, typically parylene by chemical vapor deposition, is deposited onto the paper's surface prior to the fabrication of the bottom-gate OFET structure. With the exception of recent work by Zschieschang and Klauk [12], which reported on the low voltage operation of bottom-gate OFETs that use an AlO_x /self-assembled-monolayer gate dielectric, the operational voltage of bottom-gate OFETs on paper has been on the order of tens of volts due to the use of relatively thick gate dielectric layers which lead to small capacitance density values ($< 16 \text{ nF/cm}^2$). Although bottom-gate OFETs can be engineered to display low-voltage operation,

high-mobility values and excellent short-term operational stability, the exposure of the semiconductor layer to the ambient (e.g. air or water) will eventually lead to changes of the device performance, which in the past, have been exploited to develop sensors [16], but are less desirable to develop reliable electronic circuits. For this reason, we believe that the use of a top-gate OFET geometry is particularly attractive because, as we have shown, in this geometry the organic semiconductor layer is protected from the environment while at the same time, the gate dielectric can be engineered to enable top-gate OFETs to operate at low voltage values and to display exceptional operational and environmental stability even in aqueous environments [17-20]; as well as when fabricated on plastic [21] or on cellulose nanocrystal (CNC) substrates [11]. However, reports on top-gate OFETs on paper are scarce. Recently, Mirari, *et. al.* [8] reported on dioctylbenzothienobenzothiophene (C_8 -BTBT)-based top-gate OFETs fabricated on inkjet printing paper planarized with parylene. These OFETs displayed high mobility values up to $2.5 \text{ cm}^2/\text{Vs}$ at large operational voltages on the tens of volts range. Although the transfer characteristics of these devices present no hysteresis, no systematic study was conducted on their long-term operational stability. Hence, despite great progress in recent years, there is still a need to develop approaches that will allow OFETs on paper to operate at low voltages and with good operational and environmental stability.

In this paper, we report on the realization of solution-processed top-gate OFETs fabricated on commercially-available specialty paper PowerCoat™ HD 230 from Arjowiggins Creative Papers and on their operational stability. PowerCoat™ HD 230 paper substrates, here on referred to as HD 230 paper substrates, is a 220 μm -thick ultra-smooth paper substrate, with a root-mean square (RMS) surface roughness $< 20 \text{ nm}$, designed for applications in advanced printed electronics such as high-definition patterning of microelectronics and electroplating. We

demonstrate that the use of a solution-processed buffer layer comprising of a 1:1 wt.% blend of polyvinyl alcohol (PVA) and polyvinylpyrrolidone (PVP) mixture coated leads to OFETs that display high performance and good operational stability. Blends of PVA and PVP display many desirable properties for a buffer layer since they are water-soluble, biodegradable, and low-cost materials that are highly miscible [22] and form polymer blends with very low crystallinity [23]. Top-gate OFETs fabricated on HD 230 paper display low threshold voltage values in the range of -2 to -3 V and high carrier mobility values in the range of 0.1-0.4 cm²/Vs. Furthermore, these OFETs display good operational stability, as demonstrated by highly reproducible transfer characteristics even after 1000 continuous scans. In addition, these OFETs display less than 6% on-current changes (at a drain and gate voltage value of -10 V) during DC bias stress tests for 1 h. This level of electrical performance is comparable to our previous reports on top-gate OFETs fabricated on conventional glass substrates. Finally, initial studies on the mechanical properties of these OFETs show reveal stable electrical properties during bending tests under a small strain of 0.82%.

2. OFET fabrication and characterization

Top-gate bottom-contact OFETs with the structures shown in Figure 1 (a) and (b) were fabricated on PowerCoat™ HD 230 from Arjowiggins Creative Papers. HD 230 paper substrates are 220 µm-thick and use a proprietary coating to achieve a RMS surface roughness of < 20 nm. Type-1 OFETs were fabricated directly on HD 230 paper. For type-2 OFETs, a buffer layer comprising a polyvinyl alcohol (PVA) and polyvinylpyrrolidone (PVP) (1:1 wt.%) mixture was first deposited onto the HD 230 paper substrate. The thickness of the buffer layer is 1.1 µm, measured using a stylus profilometer. Figure 1 (c) and (d) displays AFM images of bare and PVA:PVP coated HD 230 substrates. Analysis of these images reveals that bare HD 230 RMS

paper displays a surface roughness of 11 nm, consistent with manufacturer's specifications. In contrast, PVA:PVP coated HD230 paper displays an RMS surface roughness of 3 nm, which demonstrates the planarization effect of the PVA:PVP coating.

To fabricate OFET on HD 230 paper substrates, we used polydimethylsiloxane (PDMS)-coated glass to support the paper substrates during the different steps of fabrication. PDMS was prepared by mixing the Gelest OE 41 base and the cross-linker mixture at a 1:1 wt.%. PDMS films were then spin-coated onto 3.8 cm by 3.8 cm glass substrates at 2000 rpm for 60 s (acceleration: 928 rpm/s) and the films cured at 80 °C for 1 h. After PDMS was cured onto a glass substrate, a HD 230 paper substrate was adhered to its surface and secured with Kapton tape on the edges. For type-2 OFETs, a 1:1 wt.% mixture of PVA (Sigma Aldrich) and PVP (Sigma Aldrich) was dissolved in distilled water at a concentration of 7.5 wt.% (150 mg + 150 mg in 4 mL distilled water) and films were spin-coated from this solution onto the HD 230 paper substrates at 1000 rpm for 60 s (acceleration: 928 rpm/s) and followed by annealing at 60 °C for 5 min. On both types of OFETs, 50 nm-thick Ag as source/drain electrodes were vacuum-deposited through a shadow mask in a thermal evaporation system, SPECTROS from Kurt J. Lesker, followed by a 1.5 nm thick layer of Mo(tfd)₃ [24], through same shadow mask. The channel width and length ratio (W/L) is 2550 μm / 180 μm for all OFETs in this report. An organic semiconductor layer comprising a 6, 13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene) (Sigma Aldrich) and Poly[bis(4-phenyl)(2,4,6-trimethylphenyl)amine] (PTAA) (Sigma Aldrich) (1:1 wt.%) blend was then deposited by spin coating from a 30 mg/mL 1, 2, 3, 4-Tetrahydronaphthalene anhydrous, 99%, (Sigma Aldrich) solution onto source and drain electrodes. The TIPS-pentacene/PTAA solution was stirred overnight using a magnetic stirrer and spin-coated (filtered with a 0.2 μm filter) at 500 rpm for 10 s (acceleration: 500 rpm/s),

followed by 20 s at 2000 rpm (acceleration: 1000 rpm/s). The organic semiconductor film was then annealed at 100 °C for 15 min. The organic active layer was coated with by a CYTOP layer (ca. 45 nm) fabricated by spin-coating at 3000 rpm (acceleration: 10000 rpm/s) for 60 s and by annealing at 100 °C for 10 min. To achieve a thickness of 45 nm the as-purchased 9% CYTOP solution (CTL-809M) was diluted with the solvent CT-SOLV180, in a 1 to 3.5 volume ratio, to achieve a 2% CYTOP solution. After coating the organic semiconductor with CYTOP, 200 cycles of Al₂O₃ followed by a nanolaminate (NL) layer comprising 5 cycles of Al₂O₃ and 5 cycles of HfO₂ repeated 20 times, were deposited at 100 °C in a Savannah 100 ALD system from Cambridge Nanotech Inc. On top of the CYTOP/NL bilayer gate dielectric, a 100 nm of Ag gate electrodes was deposited under vacuum through a shadow mask in the thermal evaporation system, SPECTROS from Kurt J. Lesker.

The electrical characterization of all devices was conducted in a nitrogen-filled glove box with a level of O₂ and H₂O < 0.1 ppm at 25°C using an Agilent E5272A source/monitor unit. The capacitance density of the gate dielectric layer comprising CYTOP/Al₂O₃/NL was measured by an Agilent 4284A in capacitors with bottom Au and top Ag electrodes. A capacitance density of 29.4 ± 0.2 nF/cm² was extracted from measurements in nine capacitors with an area ranging from 10×10^{-3} cm² to 40×10^{-3} cm².

3. Results and discussions

Figure 2 shows representative transfer and output characteristics of type-1 (Figure 2 (a) and (c)) and type-2 OFETs (Figure 2 (b) and (d)) measured after device fabrication. Plots of $I_{DS}^{1/2}$ vs V_{GS} displayed the square law behavior expected from ideal field-effect transistors. This behavior allows extraction of the field-effect mobility value in the saturation regime by fitting the data with a square law model using a W/L of 2550 μm / 180 μm and a gate dielectric

capacitance density of $29.4 \pm 0.2 \text{ nF/cm}^2$. Type-1 OFETs displayed carrier mobility values of $3.7 \pm 2.1 \times 10^{-4} \text{ cm}^2/\text{Vs}$, threshold voltage values of $-3.0 \pm 1.9 \text{ V}$, and on/off current ratio of $2.2 \pm 1.3 \times 10^2$ with a device yield of 8/10. In contrast, type-2 OFETs displayed higher carrier mobility values of $1.7 \pm 1.1 \times 10^{-1} \text{ cm}^2/\text{Vs}$, lower threshold voltage values of $-1.4 \pm 0.2 \text{ V}$, and on/off current ratios of $4.2 \pm 4.0 \times 10^5$ with a device yield of 7/8. As demonstrated by these data, the use of a buffer layer in type-2 OFETs allows the realization of top-gate OFETs with a performance level that is comparable to that measured on devices fabricated on glass [17, 18, 20] or plastic substrates [21]. Since the surface of the HD 230 paper substrates is smooth, differences in device performance are expected to be related to differences in morphology during the formation (i.e. wetting) and phase segregation of the organic semiconductor layer. Figure 2 displays polarized microscope images, taken on reflection mode, of top-gate OFETs fabricated on bare HD 230 paper (Figure 2 (e)) and on PVA:PVP coated HD 230 paper (Figure 2 (f)). These images reveal striking differences on size and shape of the birefringent regions corresponding to TIPS-pentacene micro crystalline domains. The appearance of elongated feather-like TIPS-pentacene micro crystalline domains on OFETs fabricated on PVA:PVP coated HD 230 paper, is consequently correlated with their superior performance when compared to OFETs fabricated on HD 230 paper, displaying limited long-range crystallinity. These differences extend to the channel area, albeit they are more difficult to observe given the top-gate geometry of our OFETs. Hence, from this results it is clear that the PVA-PVP buffer layer provides improved conditions for the phase segregation and crystallization of TIPS-pentacene during the formation of the semiconductor layer.

The operational stability of type-2 OFETs was then tested by measuring the transfer characteristics (i.e. sweeping V_{GS} from 2 to -10 V) 1000 times inside a nitrogen-filled glove box.

Figure 3 (a) demonstrates stable 1000 scans of transfer characteristic of type-2 OFET. Furthermore, these OFETs were subjected to a DC bias stress at $V_{DS} = V_{GS} = -10$ V for 1 h. As shown in Figure 3 (b), the on-current of four OFETs on two substrates varies within 6% of its original value. Although these OFETs on paper, display larger device-to-device variability than what we have previously observed, this level of performance is still comparable to the one we have previously reported of top-gate OFETs using a CYTOP/ Al_2O_3 gate dielectric fabricated on glass [17, 18], plastic [21], and CNC/glycerol [11] substrates.

Bending tests were also conducted on type-2 OFETs. It is worth mentioning that these tests were conducted after storing these OFET in a nitrogen-filled glove box for 120 days. As shown in Figure 4, the transfer characteristics displayed no changes, demonstrating the good compatibility of the PVA/PVP buffer layer with the top-gate OFET structure. We should note that in the past, similar devices fabricated on bare CNC/glycerol substrates [11] displayed significant changes of their electrical properties after one month storage in a nitrogen-filled glovebox due to physical and chemical interactions between the semiconducting layer and the substrate. For the bending test in Figure 4 (a), OFETs on HD 230 paper were bended under tensile stress to a radius of curvature of 13.5 mm defined by a glass cylinder and secured to the cylinder using Kapton tape. The bending direction was parallel to the OFET channel and with a measured substrate thickness of 0.220 mm, we can calculate that OFETs were subjected to a strain value of 0.82%. As shown in Figure 4 (b), no significant changes of the transfer characteristics were observed at this bending radius. From the transfer characteristics, this representative type-2 OFET displayed a change of carrier mobility from 0.22 to 0.20 cm^2/Vs during bending, while the threshold voltage changed from -1.1 to -0.9 V, well under device-to-device variations. However, after releasing the OFETs and recovering their flat shape, the

transfer characteristics of the OFETs reveal a slight increase of the off-current which is attributed to increased gate-to-source leakage current through the dielectric layer. This failure may reveal already the onset of degradation, even if not too severe, of the ALD synthesized Al_2O_3 layer in the dielectric bilayer. Figure 4 (c) displays a small degradation of on-state current less than $1\ \mu\text{A}$ observed during the bending test, and the decreased on-state current was recovered after reflatting the paper substrate. Statistical data on type-2 OFETs during and after bending test are displayed in Table 1.

4. Conclusions

In this study, we demonstrated TIPS-pentacene:PTAA-based top-gate OFETs using a CYTOP/ Al_2O_3 /nanolaminate gate dielectric layer on PowerCoat^{TM} HD 230 paper substrates coated with a solution-processed PVA:PVP (1:1 wt.%) buffer layer. We demonstrated that these top-gate OFETs display low operating voltage values of few volts with average carrier mobility values of $1.7 \pm 1.1 \times 10^{-1}\ \text{cm}^2/\text{Vs}$, average threshold voltage of $-1.4 \pm 0.2\ \text{V}$, and on/off current ratios of 10^5 . In addition, these OFETs achieve good operational stability and can be deformed under a tensile stress to a strain of 0.82% without displaying significant changes of their electrical characteristics. Although the environmental stability has not been studied in this paper, the absence of a barrier layer underneath the OFET structure (i.e. on the substrate side) is expected to yield OFETs with relatively poor environmental stability due to the ingress of moisture and oxygen. Further studies will focus on improving the mechanical properties of the gate dielectric bilayer and on introducing an appropriate barrier layer underneath the OFET structure to insure that the environmental stability of OFET's fabricated on paper is comparable to the one we have previously reported on similar devices fabricated on glass. We believe that the level of performance achieved by top-gate OFETs reported in this work, represent a

significant step forward towards the development of OFETs on paper substrates with a stable electrical performance.

FIGURES

Figure 1. (a) OFETs on bare HD 230. (b) OFETs on PVA:PVP coated HD 230. (c) An AFM image of bare HD 230. (d) An AFM image of PVA:PVP coated HD 230.

Figure 2. (a) Transfer characteristics of the representative type-1 OFET. (b) Transfer characteristics of the representative type-2 OFET. (c) Output characteristics of the representative type-1 OFET. (d) Transfer characteristics of the representative type-2 OFET. (e) A polarized microscope image of the representative type-1 OFET. (f) A polarized microscope image of the representative type-2 OFET.

Figure 3. Operational stability test of a type-2 OFET (a) 1000 scans of transfer characteristics (b) DC bias stress for 1 h.

Figure 4. (a) A photograph of the bending test. (b) Transfer characteristics of a type-2 OFET in the bending test. (c) Output characteristics of a type-2 OFET in the bending test.

TABLES

Table 1. Summary of type-2 OFETs in the bending test.

Steps in the bending test	μ (cm ² /Vs)	V_{TH} (V)	I_{ON}/I_{OFF}	Yield
Flat paper substrate	$1.4 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.1	5.7×10^4	8/8
During bending	$1.2 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.2	4.7×10^4	8/8
After bending	$1.2 \pm 0.8 \times 10^{-1}$	-0.9 ± 0.2	1.2×10^4	8/8

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