High Mobility Multibit Nonvolatile Memory Elements Based Organic Field Effect Transistors with Large Hysteresis

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Abstract

High mobility multibit nonvolatile memory elements based on organic field effect transistors with a thin layer of polyquinoline (PQ) were reported. The devices show a high mobility of $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in the saturation region which is among the best reported for nonvolatile organic memory transistors. The multibit nonvolatile memory elements can be operated at voltage less than 100 V with good stability under continuous operation conditions and show long retention time. The different initial scanning positive gate voltages to -100 V result in several ON states, while the scanning gate voltage from -100 V to positive voltage leads to a same OFF state. The charge trapping model of electrons into the PQ layer was used to explain the origin of the memory properties.

Introduction

Organic memory elements have attracted significant interest recently due to the widespread use of portable electronic devices and its unique advantages, such as low-cost, light-weight and good compatibility to plastic or transparent substrates.[1-8] Among them, nonvolatile organic memory transistors (NOMTs) are especially desirable because of its non-destructive read-out, complementary metal oxide semiconductor architectural compatibility, and single transistor application. Since the first report by Remiens et al,[1] enormous efforts have been devoted to improve the performance of simple device structure NOMTs.[9-26] In order to meet the demands for increased data storage capacity, multi-bit memory devices (i.e., memory devices capable of storing at least 2-bit data per constituent memory cells) have been explored to replace single-bit memory devices because of the limitation of the scaling methods.[27] Guo et al. reported the first light-assisted multibit NOMT device based on pentacene/copper phthalocyanine with a polystyrene or poly(methyl methacrylate) as a modified dielectric layer.[28] However, the multibit memory devices do not show excellent field-effect performance and multibit storage ability, exhibiting a low mobility of $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for pentacene and two bits storage in a single device. In addition, the devices also need an additional light source to accomplish multibit memory, which will cost more power. This may also cause photo-oxidative degradation of the organic semiconductor. All these impede the devices to be used for practical applications. Marcus et al. also reported a single wall carbon nanotube-based FET memory element with HfO_2 as a gate dielectric with large hysteresis due to charge-trapping of HfO_2 .[29] Wang et al. have successfully controlled the threshold voltage by changing the starting gate voltage of transfer curves.[30] Herein, we will explore the feasibility of using gate voltage to control the charge trapping between the dielectric and the organic semiconductor (pentacene) to create large hysteresis for realizing multibit NOMTs. Polyquinoline (PQ) is

a commercial dielectric material with good thin film processibility, excellent thermal stability, and low moisture absorption.[31-33] More interestingly, the large difference of electron injection barrier between PQ and dielectric layer (such as SiO₂) will allow PQ to be used as a charge trapping layer between organic semiconductor and dielectric to enhance both the field-effect performance and the memory effect. To this end, a thin layer of PQ was used as the charge-trapping layer to modify the SiO₂ dielectric. The pentacene-based OFETs were fabricated. Pentacene is a highly conjugated polycyclic aromatic hydrocarbon, which has been widely studied in OFETs due to its good semiconducting behaviour. The mobilities of pentacene-based OFETs have been improved from 0.001 to 3 cm² V⁻¹ s⁻¹ by either using different deposition methods or different gate dielectric layer.[34, 35] The transfer curves of pentacene-based OFETs with the PQ modified layer show large hysteresis windows, which could be controlled by the starting gate voltage (V_{GS}). This will demonstrate the multibit nonvolatile memory elements with several ON states. The memory elements can work at voltage lower than 100 V with good stability under continuous operation and long retention time. The hysteresis comes from the modulation of the gate field by the trapped charges in the thin PQ layer.

Results and discussion

The cross-sectional view of the fabricated device structure and molecular structure of PQ are shown in Fig. 1a. The device fabrication is shown in the Experimental Section. Fig. 1b shows the output characteristics of the devices with 20 nm PQ layer that featuring good *p*-type FET behaviours. The good fitting of the current-voltage (I-V) curves to the transistor model in linear and saturation regimes are observed. The transfer characteristics of the memory elements are shown in Fig. 1c and d, and all curves were measured from the various starting source-gate voltage (V_{GS}) to -100 V in both the forward and reverse directions at a source-drain voltage (V_{DS}) of -5 V. Clear clockwise hysteresis characterized by the

reversible, positive hysteresis window ($V_{T, hysteresis} = V_{T, reverse} - V_{T, forward}$) are found for all the sweep ranges and the large shift of threshold voltage during the reverse gate sweep is observed. For the transfer curve with the starting V_{GS} of 100 V, the hysteresis window is about 70 V, which is comparable to that reported for ferroelectric FETs with poly(vinylidene fluoride/trifluoroethylene) ferroelectric copolymer as a gate insulator.[12] With the shift of the starting V_{GS} from 100 V to 0 V, the hysteresis windows decreased to lower than 10 V. The similar phenomena are also observed from $|I_{DS}|^{1/2}$ versus V_{GS} characteristics. A large hysteresis can be observed when the device operated between the depletion mode (normally “ON” at $V_{GS} = 0$) and the enhancement mode (normally “OFF”). Based on the conventional characterization equation in the linear region, the measured values of the typical field-effect mobility and on/off ratio are $0.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and 10^4 , respectively. It is interesting that all these transfer curves are parallel and the calculated mobilities are similar. This result indicates that the starting V_{GS} value does not affect the mobility of the device. Similar hysteresis can also be observed for the transfer curves in the saturation region ($V_{DS} = -100 \text{ V}$) (Fig. S1), but the hysteresis windows are smaller than those in the linear region. In addition, the ON and OFF currents are all increased while the on/off ratios are kept at 10^4 . The field-effect mobility of the saturation region was calculated to be about $1\text{-}1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is among the highest value for the reported NOMTs. The high hole mobility of the transistor is due to the good film morphology, high crystalline of pentacene, and the good interface of pentacene/PQ. The good PQ dielectric and pentacene interface also possibly contributes to the high performance of the transistor. The field-effect mobility of the transistor without PQ film in the saturation region was calculated to be $0.1\text{-}0.3 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is much lower than the one with PQ film. It is well known that the mobility in the linear region is usually lower than the one in the saturation region since the mobility in the linear region (small V_{DS}) is more drain-voltage-dependence and the saturation region mobility is expected to be more

field-dependent.[36] The small hysteresis in saturation region is because that the small amount of the electrons are trapped in PQ layer compared to that in the linear region, when the source-drain voltage is high and carriers transport is faster between the electrodes. Similar hysteresis and higher mobility can also be observed for the devices with $W/L = 28$, indicating that the channel size does not influence the hysteresis and higher mobility of the devices with PQ buffer layer (Fig. S2). AFM and XRD results demonstrated that the high mobility of the device results from the good crystallinity of the pentacene film and good interconnection of crystal domains in films (Fig. S3). The XRD pattern and AFM image of the pentacene film without PQ layer is also shown for comparison. Interestingly, the I_{DS} in the forward cycle is decreased when the starting V_{GS} goes from 100 V to 0 V while in the backward cycle, the I_{DS} is the same. This means that the devices show several different ON states but the same OFF ones. Therefore, we expect that the devices can be used as multibit memory elements.

Fig. 1. (a) Molecular structure of PQ and the cross-sectional view of NOMTs; (b) Output characteristic of pentacene-based FETs with a 20 nm PQ buffer layer. (c) $|I_{DS}|$ versus V_{GS} and (d) $|I_{DS}|_{1/2}$ versus V_{GS} characteristics of pentacene-based FETs with a 20 nm PQ buffer layer in the linear region ($V_{DS} = -5$ V, $W/L = 101$). The sweep rate is 0.5 V/s. The forward parts of the transfer curves (from positive voltage to negative voltage) are shifted to negative direction while the backward parts of the transfer curves (from negative voltage to positive voltage) overlap.

Fig. 2. (a) Calculated HOMO and LUMO orbitals of PQ. (b) Schemes for electron transfer and trapping between pentacene and PQ, where $E_{F,Si}$ and $E_{F,OSC}$ are the Fermi levels of silicon and pentacene, respectively.

To explore the origin of the large hysteresis and the hysteresis dependence on the starting V_{GS} , we have fabricated a pentacene-based OFET device using SiO_2 as insulator. However, no hysteresis was observed for the transistors without PQ buffer layer (Fig. S4). Therefore, the large hysteresis and its dependence on V_{GS} should originate from PQ buffer layer. The hysteresis of OFETs may be caused by (1) the channel/dielectric interface-induced effect, (2) the residual dipole-induced effect (due to slow polarization in the bulk organic dielectric) or (3) the effects of charges injected from the gate electrode.[37] As shown in Fig. 1c, d, the hysteresis does not reach saturation when the starting V_{GS} is

increased, so the dipolar polarization should not be the reason to cause the large hysteresis.[38, 39] In addition, given the relatively thick SiO₂ (300 nm) and the very low leakage current (10^{-10} A cm⁻²), the injected charges from the gate will not be able to contribute to the large hysteresis.[40] This was verified by the direction of the hysteresis. The similar hysteresis in the transfer curves, which become larger when the V_{GS} increased, has also been observed previously for the ambipolar, co-contacted carbon nanotube field effect transistors (CNFETs) and *p*-type organic transistors with Ferrocene/PMMA as buffer layer.[19, 41] So, the large hysteresis and dependence of hysteresis on the starting V_{GS} can be mainly ascribe the channel/dielectric interface-induced effect. Considering the chemical structure of PQ, it can find that the electron-deficient quinoline unit (Fig. 1) is more likely to play as an efficient electron trap, which means the electrons will be trapped at the dielectric interface and/or within the layer.[38, 42, 43] This made the possibility of electron trap occurred within PQ layer from the point-of-view of the structure in the dielectric layer. The sign of the trapped electrons can also be determined by comparing the on-to-off swept characteristics. The more straight line in the device with PQ layer compared to that without PQ layer in the on-to-off swept characteristics indicates the form of trapped electron in PQ layer since the on-to-off swept curve better resembles a straight line at high negative V_{gs} under electron trap model.[37, 41] It can also be demonstrated by the relationship between the threshold voltages and the starting V_{GS} during the forward sweep.

The energy barrier for the electron injection can be estimated by LUMO difference between pentacene and PQ. The electron delocalization of HOMO/LUMO energy levels was calculated by density functional theory (DFT), as shown in Fig. 2a. The HOMO and LUMO levels are calculated to be about -5.60 and -2.50 eV, respectively, and the band gap of PQ polymer is about 3.10 eV, which is comparable with previous report.[44] For SiO₂, the vacuum level is ~0.95 eV above its conduction band and its band gap

is about 8-9 eV. As shown in Fig. 2b, the energy barrier for electron injecting from LUMO of pentacene to PQ is only about 0.5 V, whereas the energy barrier for electron injecting from LUMO of pentacene to SiO₂ is about 2.05 eV.[45] The significant smaller energy barrier between pentacene and PQ will make the injection of electrons be much easier from pentacene to PQ, and thus will contribute to the large hysteresis (Fig. 2b). On the other hand, for the devices without PQ buffer layer, the higher energy barrier impedes the injection of electrons from the pentacene layer to SiO₂ at the same V_{GS} (even the electric field is higher), as result no hysteresis was observed. This is consistent to the observed phenomena. This result indicates when the devices with PQ layer are under high V_{GS} , electrons could be easily trapped by the PQ trapping layer due to the lower energy barrier between pentacene and PQ.[46, 47]

The relative amount of the electrons trapped in the PQ layer can be calculated by the threshold voltage shift in the forward direction of the hysteresis (the threshold voltage of the curve with starting V_{GS} of 0 V as the reference) as following:[48]

$$\Delta n = \frac{C_i \Delta V_T}{e} \quad (1)$$

where e , ΔV_T and C_i are the elementary charge, the shift in V_T , and the capacitance of the gate dielectric, respectively. When the starting V_{GS} shifts from 100 V to 0 V, the electric field at the interface between pentacene and PQ decreases, and the amount of electrons trapped by PQ layer also decreases, resulting in the dependence of hysteresis on the starting V_{GS} (small hysteresis at low starting V_{GS}). According to Equation 1, the electrons trapped in PQ layer were calculated to be as ca. 4.38×10^{12} , 4.06×10^{12} , 3.00×10^{12} , 2.06×10^{12} and 9.4×10^{11} for the starting voltages of 100 V, 80 V, 60 V, 40 V and 20 V, respectively. We have also fabricated the device with thicker PQ buffer layer (40 nm), which show the

similar hysteresis for their transfer curve (Fig. S5). The thicker PQ buffer layer exhibits a smaller hysteresis at the same starting V_{GS} due to the lower electrical field.

Fig. 3. (a) Write-read-erase cycles of the devices: the corresponding I_{DS} at $V_{DS} = -5$ V versus time achieved from different gate pulses. (b) The applied gate pulses versus time with writing voltage of 100 V and erasing voltage of -100 V as an example (See supporting information for other writing voltages).

The large hysteresis allows the device to function as a multibit nonvolatile memory cell, and the dynamic memory properties are depicted in Fig. 3, which shows the time evolution of the remnant conductance of the source-drain channel (i.e. the conductance at zero gate voltage). The state of the device is read at $V_{DS} = -5$ V, $V_{GS} = 0$ V. The writing voltages are 100, 80, 60 and 40 V, and the erasing voltage is -100 V. All gate voltage pulses are with the duration of 1 s. It can be observed that the remnant channel conductance is dependent on the history of the gate voltage: the remnant conductance is large after a positive gate voltage of 100 V is applied (ON-state about 9×10^{-6} A) and is small after a negative voltage of -100 V is applied (OFF-state about 2×10^{-8} A), affording an ON/OFF ratio of 10^2 . The results are comparable with the results reported by Someya et al..[49] This indicates that the memory devices are written by applying positive voltage and erased by applying negative voltage pulse. As the remnant conductance results from the trap of charges in PQ, we can conclude that electrons are trapped in PQ for the positive writing voltage and negative erasing voltage, which coincides with the results above. Similar results are obtained with different writing voltages (80, 60 and 40 V) and erasing voltage at -100V. The ON-state currents are

proportional to the writing voltage and no decay can be observed (the currents remains constant): the ON-state current is 9×10^{-5} A for the writing voltage of 100 V and is 6×10^{-8} A for the writing voltage of 40 V. This demonstrates that the devices can be used as multibit NOMTs. For the device with thicker PQ layer (40 nm), the writing/erasing time is much longer and the ON/OFF ratios are much lower than those of the device with 20 nm PQ layer. The inferior performance can be explained by lower electrical field, resulting in the uneasy trap of electrons, which coincide with the results and analysis above.

To evaluate the ability of the memories to retain information, the retention times of ON and OFF states were recorded and shown in Fig. 4a. Both the ON- and OFF-current states were measured at $V_{DS} = -5$ V and $V_{GS} = 0$ V in the dark after applying different writing and erasing bias for 1 s, respectively. All the currents have a non-exponential decay during the measurement, with a relatively subtle initial decay in the beginning then following with a stronger decay. Nevertheless, the devices exhibit good retention characteristics (10^3 s) with extrapolated retention times of more than 10^5 s. The retention times are comparable with those of NOMT and organic unipolar memory reported,[49, 50] which indicates a reasonably stable behavior in capability of information storage. At the beginning, the intrinsic holes will compensate the deeply trapped charges until the holes are nearly exhausted, leading to a relative subtle initial decay. Then, the remaining deeply trapped charges are gradually compensated by the carrier pairs which is slowly generated in PQ dielectric layer and will supply a small amount of holes, as a result a stronger decay is observed.[30, 48, 51] We have also investigated how the memory devices perform under the continuous writing and erasing pulses (Fig. 4b) to study its stability. The ON and OFF currents do decay up to more than 300 cycles, and then the ON/Off current ratio is constant at 10^2 up to more than 300 cycles. Beyond that, the ON current began degrading while the OFF current is still constant. Although degradation was observed, good ON and OFF state more than 1000 times can be still achieve for our devices, which is sufficient for unambiguous read-out and comparable to the previous reported results.[12, 28, 49]

Even after 1000 programmed cycles, the devices still show similar hysteresis, but the hystereses are smaller and the ON-currents are lower (Fig. S6). Further experiments are required to explain and prevent the decline.

Fig. 4. (a) Retention properties of different write and erase states recorded under $V_{DS} = -5$ V, $V_{GS} = 0$ V, for 2000 s. (b) The ON- and Off-state drain currents at $V_{DS} = -5$ V and zero gate bias as a function of the number of applied gate voltage sweeps.

The gate voltages of ± 100 V were applied for 1 s.

In conclusion, we have reported the high-performance multibit nonvolatile memory elements based on OFETs with a thin PQ modifying layer. The devices show the high mobility of as high as $1.5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ in the saturation region. This value is one of the highest reported for NOMTs. The different initial scanning positive gate voltages shift the transfer curves, and then it is easy to accomplish the multibit nonvolatile memory. The different positive writing voltages (from 100 to 20 V) result in several ON states, while the erasing voltage (-100 V) leads to a same OFF state. The memory devices can be operated at voltages lower than 100 V with good stability under continuous operations (more than 1000 cycles). Further decreasing the operating voltages will be possible by optimizing the device structures, interface engineering and materials, etc. The charge trapping of electrons into the PQ layer was used to explain the origin of the multibit memory properties. The multibit memory elements have great potential to be used in the portable electronic devices.

Experimental

OFETs were fabricated with a top-contact configuration. An n-type Si wafer and 300 nm thick layer of thermally grown SiO₂ were used as the gate and gate insulator, respectively. The substrates were cleaned in water, acetone and isopropyl alcohol. After that, the substrates were put into a chamber for oxygen plasma for 3 min. Then, the PQ buffer layer was spin-coated onto the surface of SiO₂ and the final thickness was measured to be about 20 nm and 40 nm by AFM. After that, pentacene was deposited onto the substrates by high vacuum evaporation at a rate of 0.4 Å s⁻¹ from a resistively heated quartz crucible at 4 × 10⁻⁷ Torr to achieve a total film thickness of 50 nm. Subsequently, Au films (50 nm) as drain and source electrodes, were deposited on the organic layer through a shadow mask. For a typical device, the channel length (*L*)/width (*W*) of the OTFT were 28 (*L* and *W* were 55 and 1550 μm) and 101 (*L* and *W* were 89 and 900 μm), respectively. All devices were characterized with an Agilent 4155B semiconductor parameter analyzer under ambient conditions without any precautionary measures being taken to isolate the devices from exposure to ambient oxygen and moisture. The mobility of the devices in the saturated regime was extracted from the following equation:

$$I_{DS} = C_i \mu (W / 2L) (V_{GS} - V_T)^2$$

where *I_{DS}* is the drain current, *C_i* is the capacitance per unit area of the gate dielectric layer, and *V_{GS}* and *V_T* are the gate voltage and threshold voltage, respectively. The threshold of the device was determined from the relationship between the square root of *I_{DS}* at the saturated regime, and *V_{GS}* was determined by extrapolating the measured data to *I_{DS}* = 0.

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