Si/Sb superlattice-like thin films for ultrafast and low power phase change memory application

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Abstract: After compositing with Si, the superlattice-like (SLL) Si/Sb thin film had higher crystallization temperature (~ 231 °C), larger crystallization activation energy (2.95 eV), and better data retention ability (126 °C for 10 years). The crystallization of Sb in SLL Si/Sb thin films was restrained by the multilayer interfaces. The reversible resistance transition could be achieved by an electric pulse as short as 10 ns for [Si(22nm)/Sb(2nm)]₂-based PCM cell. A lower operation power consumption of 0.02 mW and a good endurance of 1.0×10^5 cycles was achieved. In addition, SLL [Si(22nm)/Sb(2nm)]₂ thin film showed a low thermal conductivity of 0.11 W/(m·K).

Keywords : superlattice-like, high speed, low power, phase change memory

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As a promising next generation nonvolatile memory, phase change memory (PCM) has attracted much attention in recent years due to its outstanding performance, such as high density, low power consumption, good endurance, fast programming capability, and fabrication compatibility with complementary metal-oxide-semiconductor (CMOS) [1, 2]. The basic principle is the reversible phase change between the amorphous (showing high resistivity) and crystalline states (showing low resistivity) by current Joule heating. The two resistance states with enormous differentiation can be used as logic “0” and “1” to storage data [3].

The large-scale application of PCM has been hindered by the two prominent issues, the slow phase change speed and high operation power consumption [4, 5]. The characteristics of phase change materials have deep influence on the performance of PCM, thus many phase change materials have been studied. $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST) is now the most widely used phase change material because it has the business application in optical storage [6]. However, the poor data retention (85 °C for ten years) and slow switching speed in SET and RESET operation processes limit its application in future mass storage [7]. It is reported that the PCM device based on GST material is difficult to have an entire operating window when the width of the voltage pulse is shorter than 100 ns, which is insufficient to satisfy the requirement of dynamic random access memory (DRAM) (~10 ns) [8]. Recently, Sb-rich phase change materials, such as W-Sb-Te [9], Si-Sb-Se [1] and Cu-Sb-Te [10], have been proved to have faster switching characteristics because of their growth-dominated crystallization mechanism. Compared with bulk materials, the phase change materials with superlattice-like (SLL) structures exhibit a higher working speed and a lower programming current due to their much lower thermal conductivity [11]. Moreover, the SLL phase change materials can combine the phase change performance of different composite layers to obtain an excellent comprehensive property. In this work, two elemental materials of Si and Sb were used to prepare SLL Si/Sb thin films. Their potential PCM application was evaluated by using thermal and electric characterizations.

SLL Si/Sb thin films with different periods and thickness ratios, as well as monolayer Sb thin film, were deposited on 0.5 mm thick oxidized Si (100) wafers by using a radio-frequency (RF) magnetron sputtering system at room temperature. Total thickness of the thin films was set to be

about 50 nm. The thickness of each individual layer was controlled by the deposition time. Prior to the growth of SLL thin films, the deposition rates of Si and Sb single layers were pre-determined. Thickness of the films was measured by using an Alpha-Step 500 profiler (Tencor Instrument). All deposition processes were carried out in an Ar atmosphere at a pressure of 0.2 Pa, with a flow of 30 sccm and an RF power of 20 W. The substrate was rotated at an autorotation speed of 20 rpm to guarantee the deposition uniformity.

In-situ temperature-dependent resistance (R - T) of the samples was performed in Ar atmosphere using a custom-made two-point-probe setup to obtain the phase-change details by a TP 94 temperature controller (Linkam Scientific Instruments Ltd, Surrey, UK). The activation energy for crystallization (E_a) was estimated by measuring the resistance of samples at different heating rates using the Arrhenius equation. The crystalline phases of the films were analyzed by X-ray diffraction (XRD, Rigaku D/MAX 2550V) with Cu K_α radiation in the 2θ degree range from 20° to 60° , with a scanning step of $1^\circ/\text{min}$. In order to measure local thermal conductivity, the so-called 3ω method was set up and integrated with an atomic force microscope to probe the nanoscale thermal property. The power-current (P - I), resistance-voltage (R - V) and reversible switching properties of PCM cells based on GST and SLL Si/Sb thin films were measured by a Tektronix AWG5012B arbitrary waveform generator and a Keithley 2602A parameter analyzer.

Figure 1 showed the R - T curves of SLL Si/Sb and monolayer Sb thin films at a constant rate of $10^\circ\text{C}/\text{min}$. Initially, the resistance of all amorphous SLL Si/Sb thin films decreased slowly with the increase of temperature due to a thermally assisted trap-limited conduction [12]. Then, a quick drop of resistance followed which was associated with the transformation of amorphous to crystalline state. The transform temperature was defined as the crystallization temperature T_c . As shown in Figure 1, a tremendous resistance decreasing of near two orders of magnitude was achieved for all SLL Si/Sb thin films, which could insure the enough discrimination in read/write operation. By contrast, no obvious resistance change in heating process was observed for the pure Sb thin film, which indicated that some Sb crystalline phase could have formed in depositing process due to its poor amorphous thermal stability. According to the measurement, the T_c for $[\text{Si}(1\text{nm})/\text{Sb}(5\text{nm})]_8$ was 137°C . With the increasing thickness ratio of Si to Sb in SLL Si/Sb thin films, T_c increased gradually to 231°C of $[\text{Si}(18\text{nm})/\text{Sb}(1\text{nm})]_3$. Generally, the thermal stability of

amorphous film could be roughly evaluated through the crystallization temperature T_c . Obviously, more Si elements greatly improved the amorphous stability of Sb film. In addition, the resistance of crystalline state increased from $2 \times 10^2 \Omega$ of Sb to $9 \times 10^4 \Omega$ of $[\text{Si}(18\text{nm})/\text{Sb}(1\text{nm})]_3$, which was helpful to reduce the driving current for the reset operations of PCM.

The activation energy for crystallization was a good estimate of the archival life stability of an amorphous phase-change material [13]. The crystallization temperature increased with increasing of heating rate from 10 to 40 °C/min because there was insufficient time for crystallization and nucleation to take place at a faster heating rate (not shown here). The activation energy for crystallization was calculated from a Kissinger plot [14]:

$$\ln[(dT/dt)/T_c^2] = C + E_a/(k_b T_c) \quad (1)$$

Where dT/dt was the heating rate, T_c was the crystallization temperature, C was a constant, E_a was the activation energy for crystallization, and k_b was Boltzmann's constant. Figure 2a showed the Kissinger plots of $\ln[(dT/dt)/T_c^2]$ versus $1/T_c$ for the SLL Si/Sb thin films. The E_a of $[\text{Si}(1\text{nm})/\text{Sb}(5\text{nm})]_8$ film was only 1.47 eV. After compositing with Si, the E_a of Si/Sb thin films increased significantly. Most of all, the E_a of $[\text{Si}(22\text{nm})/\text{Sb}(2\text{nm})]_2$ and $[\text{Si}(18\text{nm})/\text{Sb}(1\text{nm})]_3$ films increased to 2.48 and 2.95 eV, respectively, which were all larger than that of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ film, whose E_a was 2.28 eV [15]. Therefore, the thermal stability of Sb film was enhanced by compositing with Si.

Data retention capability, generally estimated by extrapolation of the isothermal Arrhenius plot, was a very important parameter of PCM devices [16]. Isothermal change in time-dependent resistance at different temperatures was employed to evaluate the data retention of SLL Si/Sb thin films. The failure time was defined as the time when the resistance reaches half of its initial value at a specific isothermal temperature. The inset in Figure 2b showed that the failure time of $[\text{Si}(22\text{nm})/\text{Sb}(2\text{nm})]_2$ at 175, 170, 165 and 160 °C was 72, 395, 1902 and 4997 s, respectively. That is, in lower isothermal temperature, the phase change material need more time to accumulate enough energy for crystallization. The plot of logarithm failure time vs. $1/(k_b T)$, which fits a linear Arrhenius relationship due to its thermal activation nature, can be described as [17]

$$t = \tau_0 \exp[E_c/(k_b \times T)] \quad (2)$$

where t , τ_0 , k_b , and T are failure time, the pre-exponential factor depending on the material's

properties, Boltzmann's constant and absolute temperature of concern, respectively. The 10-year lifetime for SLL Si/Sb thin films increased from 71°C of [Si(1nm)/Sb(5nm)]₈ to 126 °C of [Si(18nm)/Sb(1nm)]₃. From this perspective, SLL Si/Sb thin films possess better reliability of the resistance state to meet the application of data storage at elevated temperature.

Figure 3a and 3b showed the XRD patterns of pure Sb and SLL [Si(22nm)/Sb(2nm)]₂ thin films, respectively. In the as-deposited sample of pure Sb thin films, a broad diffraction peak (012) could be seen in Figure 3a. It indicated that the crystallization had happened in as-deposited Sb thin film, which was in accord with the result of Figure 1. With the increasing of annealing temperature, the crystal grains further grew with the width of peak (012) decreasing and appearing of Sb (110) and (202) diffraction peaks [18]. Being different from pure Sb material, no diffraction peaks were observed in the SLL [Si(22nm)/Sb(2nm)]₂ thin films in Figure 3b, indicating an amorphous nature. The first appearance of two mild humps (003) and (015) was at the temperature 150 °C, which demonstrated its better amorphous thermal stability than pure Sb material. And the intensity of diffraction peak Sb (012) observed in the SLL [Si(22nm)/Sb(2nm)]₂ thin film was much weaker than that of pure Sb. This indicated that the crystallization of Sb was restrained by the adjacent Si interfaces. The (012) peak in Figure 3b has moved a little to a lower angle, which could be ascribed to the influence of Si inclusion and interface stresses. Besides, no Si diffraction peaks were observed. It manifested that Si existed in amorphous state, which was conducive to improve the stability of Sb materials.

PCM cells based on SLL [Si(22nm)/Sb(2nm)]₂ thin films were fabricated to test and verify their electrical properties using 0.18 μm CMOS technology. The cross sectional transmission electron microscopy image was shown in the inset in Figure 4b. A 20-nm-thick TiN layer was deposited so as to improve the interface between the phase change layer (PCL) and the top electrode (Al). Figure 4 showed the Power-Current (*P-I*) and reversible switching characteristics of the [Si(22nm)/Sb(2nm)]₂-based cell devices. The *R-V* curves, shown in the inset of Figure 4a, exhibited a reversible switching phenomenon between the SET and RESET states. The GST-based

PCM device could achieve a stable operation window with the pulse width 500 ns. However, it was difficult to switch in the 100 ns pulse. By contrast, the [Si(22nm)/Sb(2nm)]₂-based cell could easily have the resistance switching with the pulse width 10 ns. The result indicated that SLL [Si(22nm)/Sb(2nm)]₂ had a faster switching speed than GST. This is ascribed to the result of the precipitation of Sb crystallites. Sb is characterized by an explosive crystallization which is a thermal process with the heat that is released at the crystallization front serving to drive the crystallization of the surrounding amorphous regions further [19, 20]. Sb crystallite may serve as a template for subsequent crystallization to reduce the crystallization time of [Si(22nm)/Sb(2nm)]₂ [21, 22].

In order to evaluate the power consumption, the *P-I* curves of SLL [Si(22nm)/Sb(2nm)]₂ and GST were measured. The largest power for [Si(22nm)/Sb(2nm)]₂-based PCM device was 0.02 mW, which was much lower than that of GST (1.22 mW). Therefore, a lower power consumption was achieved for SLL [Si(22nm)/Sb(2nm)]₂ thin film. Moreover, the reversible switching up to 1.0×10^5 cycles without failure, shown in Figure 4b, was realized for [Si(22nm)/Sb(2nm)]₂-based device cell. The good endurance character further demonstrates the practicability of SLL Si/Sb thin films in PCM devices.

The thermal conductivity of the phase-change film has a great influence on the power consumption of PCM cells [23]. In this study, scanning probe microscopy (SPM) was used to investigate microstructures and local thermal conductivity properties of various materials and devices in nanoscale [24]. Based on SPM, scanning thermal microscopy (SThM) was developed to give simultaneous surface topography image and thermal property image of materials with micro or submicrometer spatial resolution. Monolayer Si, Sb, and SLL [Si(22nm)/Sb(2nm)]₂ thin films were used as thermal conductivity measuring. The results showed that the thermal conductivity of SLL [Si(22nm)/Sb(2nm)]₂ thin film is 0.11 W/(m·K), which was much lower than that of

monolayer Si(0.56 W/(m·K)) and Sb(2.53 W/(m·K)), respectively. A low thermal conductivity can facilitate reducing heat dissipating, thus the heating efficiency is improved. Therefore, a low thermal conductivity of SLL structure are believed to play a part in decreasing the power consumption of PCM devices.

In summary, SLL Si/Sb material was investigated for the use as an appropriate phase-change material in PCM. Compared with pure Sb, SLL Si/Sb materials have better amorphous thermal stability ([Si(22nm)/Sb(2nm)]₂: T_c 185 °C, E_a 2.48 eV; [Si(18nm)/Sb(1nm)]₃: T_c 231°C, E_a 2.95 eV). The $T_{10\text{-year}}$ of [Si(22nm)/Sb(2nm)]₂ and [Si(18nm)/Sb(1nm)]₃ materials reached to 110 and 126 °C, respectively. The reversible resistance transition was achieved by an electric pulse as short as 10 ns for [Si(22nm)/Sb(2nm)]₂. Compared with GST, the [Si(22nm)/Sb(2nm)]₂-based PCM device had a lower power of 0.02 mW. The reversible switching of 1.0×10^5 cycles was achieved. The SLL [Si(22nm)/Sb(2nm)]₂ had a lower thermal conductivity 0.11 W/(m·K). These results demonstrate that SLL Si/Sb material is a promising candidate for low power and high-speed PCM applications.

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Figures and captions

Figure 1. The temperature dependence of resistance for SLL Si/Sb thin films at a constant rate of 10 °C/min.

Figure 2. (a) The Kissinger plots of $\ln[(dT/dt)/T_c^2]$ vs. $1/T_c$ for the SLL Si/Sb thin films. (b) Arrhenius plots of data retention showing extrapolated temperatures of 10-year data retention for SLL Si/Sb thin films. Inset shows the normalized resistance of SLL [Si(22nm)/Sb(2nm)]₂ thin film as a function of annealing time at various temperatures.

Figure 3. XRD pattern annealed at different temperature for (a) pure Sb thin film, (b) SLL [Si(22nm)/Sb(2nm)]₂ thin films.

Figure 4. (a) *R-V* characteristics of the cell devices based on GST and SLL [Si(22nm)/Sb(2nm)]₂ thin films. Inset shows the *I-V* curve for [Si(22nm)/Sb(2nm)]₂-based PCM cell. (b) the reversible switching of [Si(22nm)/Sb(2nm)]₂-based cell devices. Inset shows the cross-sectional TEM images of PCM cell device.

Figure 1

Figure 2

Figure 3

Figure 4

Graphical abstract

After compositing with Si, the superlattice-like (SLL) Si/Sb thin film had higher crystallization temperature ($\sim 231^\circ\text{C}$), larger crystallization activation energy (2.95 eV), and better data retention ability (126°C for 10 years). The crystallization of Sb in SLL Si/Sb thin films was restrained by the multilayer interfaces. The reversible resistance transition could be achieved by an electric pulse as short as 10 ns for $[\text{Si}(22\text{nm})/\text{Sb}(2\text{nm})]_2$ -based PCM cell. A lower operation power consumption of 0.02 mW and a good endurance of 1.0×10^5 cycles was achieved.