Graphical Abstract (for review)

Substrate Configuration, Bifacial CdTe Solar Cells Grown Directly on Transparent Single Wall Carbon Nanotube Back Contacts

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Abstract

Substrate configuration CdTe/CdS solar cells were fabricated directly on a 25 nm thick single wall carbon nanotube (SWCNT) back contacts using a high temperature, commercial deposition process. No copper was introduced to facilitate the formation of an ohmic back contact at the back of the device. The champion device had an efficiency of 6.5%. The thin SWCNT layer allowed the device to be illuminated through the back contact, and a comparison of the device performance with front and backside illumination revealed several novel features of the SWCNT back contact. Our findings indicate that SWCNT films may be useful as a recombination layer contact for bifacial solar cells, photovoltaic windows, or two-terminal thin-film tandem solar cells.

1. Introduction

With a direct band gap of 1.45 eV and a high absorption coefficient, cadmium telluride is an ideal absorber material for thin film photovoltaic (PV) devices.[1] Recently, record efficiencies were reported for both research scale devices and large area modules at 22.1%[2] and 18.6%, [3] respectively. All commercial CdTe modules are manufactured in the superstrate configuration in which the n-type CdS window and p-type CdTe absorber layers are sequentially deposited on n-type transparent conducting oxide (TCO)-coated glass plates. The superstrate configuration enables the delicate processing required for Cu doping and back contact formation to be done last, after all other high temperature depositions and any necessary processing steps have been completed. This approach leads to the highest efficiency CdTe devices and allows the copper profile, which has also been linked to the net-acceptor profile,[4, 5] to be controlled to achieve long-term stability and a low levelized cost of energy production.[6, 7]

Despite the success of the superstrate configuration, fabrication of devices in the *substrate* configuration could have several advantages. For instance, after deposition of the CdTe absorber layer directly on the back contact, the junction interface and top layers of the cells are accessible for potential control over junction optimization as well as improving light transmission into the device. The substrate configuration allows consideration of the use of flexible thin metal foils which could enable high speed, low cost, roll-to-roll processing. Unfortunately, it is difficult to fabricate high efficiency devices in the substrate configuration due to materials compatibility issues associated with forming a stable, low resistance electrical back contact.

The first reported substrate configuration CdTe device was prepared on transparent conducting oxide (TCO) coated glass as part of a thin-film tandem device structure and had an efficiency of 5.5%.[8] In an effort to improve the back contact behavior, Singh *et al.* evaporated thin Cu and Te layers on a flexible Mo substrate prior to CdTe evaporation, and obtained a best cell efficiency of

5.3%.[9]. The device efficiency was limited by a poor electrical back contact and/or Cu diffusion into the front of the device as evidenced by rollover in the forward bias portion of the current density-voltage (J-V) curve.[10, 11] In an effort to reduce the back contact barrier, Matulionis *et al.* sputtered an N-doped ZnTe layer on a Mo substrate prior to sputter deposition of CdTe. Although rollover was still observed in the J-V characteristic, an efficiency of 7.8% was reported.[12] The introduction of Cu in the form of a sputtered Cu_xTe buffer layer reduced the rollover in the J-V curves for CdTe devices grown by close-space sublimation, and an efficiency near 11% was obtained.[13] More recently, a 13.6% substrate configuration device was made when Cu was diffused into a CdTe layer that had been deposited on a Mo/MoO_x/Te back contact stack.[14] Devices in the same configuration without Cu had efficiencies below 1%, and the difference in efficiency was attributed to an optimized p-type carrier density in the CdTe. However, analysis of the composition profile revealed that, in addition to doping the CdTe, Cu had segregated at the back of the device. This suggests that an interfacial Cu_xTe layer may have formed, which would reduce the back contact barrier.[10] It is important to note that all reports of substrate configuration devices to date have shown that Cu is required to achieve even moderate energy conversion efficiencies.

Although additional Cu introduction at the back contact is also typically required to fabricate high efficiency superstrate configuration devices, we recently demonstrated that the need for additional Cu can be avoided through the use of a single wall carbon nanotube (SWCNT) back contact interface layer.[7] We subsequently showed that CdTe and CdS films deposited directly onto SWCNT layers using a high temperature, commercial vapor transport deposition (VTD) process [15] were very similar in grain structure and morphology to films that were deposited on TCO coated glass.[16]

In this contribution, we examine the photovoltaic performance of CdTe/CdS devices in the substrate configuration that were grown on thin, partially transparent SWCNT back contact interface layers by VTD. No Cu was purposefully introduced, and an efficiency of 6.5% was obtained. The use of a transparent SWCNT layer allowed the performance to be compared under both frontside (i.e.

through the CdS) and backside (through the SWCNT back contact) illumination. Interestingly, rollover in the J-V characteristics was observed when the cell was illuminated through the CdS window layer, but not when illumination was through the back contact. Device modeling was performed to aid in understanding the experimental results, and several unique aspects of the SWCNT back contact were revealed. In particular, the data suggests that SWCNT films can act as a recombination layer contact that may be useful in bifacial solar cells and two-terminal thin-film tandems.

2. Materials and Methods

SWCNTs of mean diameter ~ 1.2 nm were produced by a modified laser vaporization technique [17] and purified using the process developed by Nishide *et al.* [18] SWCNT materials were sonicated for 30 min. in sodium dodecyl sulfate ($>99.0\%$; P212121, LLC) using a probe sonicator to produce surfactant stabilized solutions. The average tube length was 500 nm [7] and the semiconducting (s-) and metallic (m-) SWCNTs were present in the natural ratio ($\sim 2:1$). [19] SWCNT films (25 nm thick, as determined by optical measurements [20]) were formed on mixed cellulose esters membranes (0.22 μm pore size, 47 mm diameter; Zefon International) by vacuum filtration. Several circular SWCNT films were transferred onto the surface of the TEC 15M coated glass plates (Pilkington NA) using the procedures developed by Wu *et al.* [21] TEC 15M coated glass plates were used for our study because they are commonly used for the fabrication of superstrate configuration modules in this deposition reactor and were readily available. Note that TEC 15M is comprised of ~ 330 nm of F-doped SnO_2 (n-type carrier concentration of $\sim 5 \times 10^{20} \text{ cm}^{-3}$) that is capped by ~ 100 nm of intrinsic SnO_2 .

The 60 cm by 120 cm TEC 15M coated glass plates were held vertically and transported through a production scale reactor. Superstrate devices are normally grown in the VTD reactor by pre-heating the TEC 15M glass to the deposition temperature in He gas, and then depositing CdS and CdTe at pressures below ambient sequentially in consecutive heated zones. To deposit CdTe first, as required for substrate configuration devices, the CdS feed was turned off while the zone temperatures were maintained at 570 °C. After deposition of ~ 4.5 μm of CdTe, as determined by Dektak

profilometry, the plates were translated through a cooling zone, unloaded from the end of the coating line, and reloaded at its start. During a second pass, also at 570 °C, the CdTe feed was turned off, the CdS feed was turned on, and ~200 nm of CdS was deposited. Interestingly, the CdTe thickness was reduced to ~3.3 μm after the second pass through the coater, presumably due to CdTe reevaporation.[22]

After deposition of the CdTe/CdS stack, the larger glass substrate was cut into 50 mm x 50 mm squares that included 47 mm diameter SWCNT films. Methanol saturated with CdCl₂ (anhydrous 99.99%; Alfa Aesar) was applied by dropper to these samples and allowed to dry. These samples were then processed using a standard protocol that has been developed for superstrate configuration devices (heating to 387 °C for 45 minutes in a graphite box purged with flowing dry air). After cooling, excess CdCl₂ was removed by repeated rinsing in methanol. Devices were completed by sputtering 80 nm of intrinsic zinc oxide (IZO) at room temperature and 800 nm of aluminum doped zinc oxide (AZO) on a 250 °C substrate through a mask that produced circular devices with an area of $0.0755 \pm 0.003 \text{ cm}^2$ as determined by photography and image analysis. Both depositions were performed under 2 mTorr Ar pressure, at an rf power of 80 W, using 2" diameter targets. The thicknesses were determined using Dektak profilometry on a witness glass slide. The IZO and AZO layers had resistivities of $1 \times 10^9 \Omega\text{-cm}$ and $8.7 \times 10^{-4} \Omega\text{-cm}$, respectively, and the IZO/AZO stack had a sheet resistance of $35 \pm 3 \text{ Ohms}/\square$ as determined by four point probe measurements on witness glass slides.

The light/dark J-V characteristics were obtained with a system (PV Measurements IVQUE8-C) consisting of a Keithley 2440 source measurement unit and a Newport model 91195A Class A solar simulator. A custom LabVIEW program was used to interface with the source measurement unit. The light intensity at the plane of the device was adjusted to yield 1000.0 W/m² using a Si reference solar that was calibrated by Newport Corporation. Low light intensity measurements were performed by installing neutral density filters (Thor Labs) between the light source and the cell. External quantum

efficiency (EQE) measurements were obtained from 300 to 900 nm (PV Measurements IVQUE8-C) without a light bias, as is typical for CdTe devices in the literature. We found good agreement, within 5%, when the measured short circuit current was compared to the value determined by multiplying the EQE response by the solar simulator's lamp spectrum and integrating. The surface morphology of the film was measured prior to IZO/AZO deposition using scanning electron microscopy (SEM, Hitachi S-4800).

3. Results and Discussion

Figure 1a shows the J-V photoresponse from a representative CdTe/CdS device that was formed by VTD on a 25 nm thick SWCNT back contact interface layer on a TEC 15M substrate. The average efficiency for 15 devices was 5.8%, with a best cell efficiency of 6.5%. For comparison, a superstrate device prepared with the same deposition system and processed similarly exhibited an efficiency of 13% with a SWCNT/Au back contact (see Supplementary Information). Figure 1a also shows the J-V photoresponse for a device that was constructed directly on TEC 15M without the intervening SWCNT layer. In this case, very low V_{oc} and short circuit current (J_{sc}) values were found after $CdCl_2$ processing, and the device efficiencies were below 1%. Clearly, the SWCNT layer is essential for good performance in this device configuration. Without any $CdCl_2$ treatment, device efficiencies were also less than 1% (data not shown). The $CdCl_2$ treatment is known to promote grain growth and grain boundary passivation, and can improve the quality of the CdTe/CdS junction.[1] Clearly, it is also necessary to achieve reasonable performance in these devices. The device parameters and statistics are shown in Table 1. Figure 1b shows the external quantum efficiency for a device constructed on the SWCNT back contact interface layer. The quantum efficiency curve looks quite similar to data that would be expected from a conventionally grown superstrate device. The large loss of photocurrent between 400 and 500 nm is consistent with the thick CdS layer used in these samples.

The substrate configuration devices built on the SWCNT interface layers show substantial rollover in the forward bias portion of the J-V curve (Fig. 1a). This feature adversely impacts the

power conversion efficiency and is normally associated with the presence of a second diode that opposes the flow of majority carriers (holes) out the back of the device.[10, 11] The behavior cannot be attributed to the SWCNT/CdTe interface since SWCNT and Au/SWCNT back contacts have been previously shown to make low barrier, Cu-free electrical back contacts to CdTe solar cells.[7] In contrast, the interaction between SWCNTs and the n-SnO₂/i-SnO₂ stack that comprises TEC 15M is completely unknown. To better understand the electrical properties of the TEC 15M/SWCNT/CdTe stack at the back of the device we employed SCAPS modeling software.[23] Because the SWCNT layer is rigorously undoped after heating to 570 °C in He,[24] the TEC 15M/SWCNT/CdTe stack was modeled as a series of n-i-i-p layers. The semiconductor and TCO layers were modeled with typical parameters,[25-27] and the SWCNT layer was considered to be an undoped semiconductor layer with a bandgap of 0.7 eV and an electron affinity of 4.65 eV, following our previous work.[7] The equilibrium band diagrams for TEC 15M/SWCNT/CdTe/CdS/IZO/AZO devices were calculated in the dark for low (Fig. 2a, $p = 1 \times 10^{12} \text{ cm}^{-3}$) and moderate (Fig. 2b, $p = 5 \times 10^{14} \text{ cm}^{-3}$) CdTe dopant densities. The low value corresponds to as-deposited, high purity CdTe that has not been exposed to significant copper, while the moderate value accounts for the possibility that copper may have been inadvertently introduced despite our use of high purity materials and chemicals. We consider the latter case explicitly because we measure relatively high efficiencies in these Cu-free devices while others have reported very low efficiency substrate configuration devices when copper was excluded during fabrication.[14]

In the case of moderate CdTe doping (Fig. 2b), there is a large potential energy barrier for majority carrier holes to exit the rear of the device due to band bending in the CdTe, while no such barrier is found for the nearly intrinsic case (Fig. 2a). This energy barrier could be the source of the rollover in the J-V characteristic, but experiments in which the illumination was directed through the TEC 15M substrate indicated that the dopant density is indeed low and that the band diagram of Fig. 2a is most appropriate (*vide infra*). Moreover, as indicated previously, no rollover was observed for

Au/SWCNT contacts to Cu-free devices.[7] Consequently, we ascribe the rollover to a potential energy barrier for hole transport from the SWCNT to the TEC 15M. Note that the 100 nm i-SnO₂ layer that is part of the TEC 15M stack can interdiffuse with deposited CdS during the normal high temperature device processing that is used for superstrate devices,[28] while such interdiffusion is not expected in the present case because the CdTe and i-SnO₂ layers are physically separated by the SWCNT layer. Thus, the undoped oxide layer may impose a barrier to charge transport, and give rise to the observed rollover. Unfortunately, this speculation could not be tested in the context of the SCAPS modeling; the J-V curve and recombination/generation rate calculations diverged due to the complexity of the band structure in the modeled devices.

Once the device model was simplified by removing the SWCNT layer, the J-V characteristics could be calculated. The efficiency was calculated to be approximately zero when the CdTe layer was directly in contact with TEC 15M, which is consistent with the experimental finding that the SWCNT layer must be present for good PV performance. For completeness, we also considered the possibility that m-SWCNTs, rather than the s-SWCNTs, controlled the back contact energetics.[7] In this case the rear contact was modeled as a metal with a work function of 5 eV. Once again, the simulated J-V performance indicated very low efficiency (< 1%). Note that the low efficiency values that were calculated for the various simplified back contacts were independent of the CdTe carrier concentration for the range that was examined (1×10^{12} to $5 \times 10^{14} \text{ cm}^{-3}$). In general, in all cases, the devices without SWCNTs were dominated by the deleterious effects associated with the TEC 15M/CdTe back interface.

More experimental insight was gained by illuminating the device through the partially transparent TEC 15M/SWCNT back contact. The combination of reflection/absorption associated with the TEC 15M/soda-lime glass substrate and additional absorption in the 25 nm SWCNT film allowed approximately 60% of the incident spectrum to pass through to the CdTe over the wavelength range of 400 to 900 nm. Figure 3a and b show the J-V and QE data, respectively, for representative devices. In addition to data for a 200 nm CdS layer prepared by VTD, data is also shown for a CdS window

prepared by two chemical bath depositions (CBD) of 80 nm with an intervening liquid CdCl_2 treatment, following the work of Gretener *et al.*[29] The net thickness of the CdS layer in this case was ~ 100 nm, as determined from EQE measurements (data not shown). The best device efficiencies with back-side illumination were 0.78% and 1.76% for the 200 nm and 100 nm CdS devices, respectively. The devices with 100 nm of CBD CdS showed higher efficiencies with backside illumination primarily due to significantly higher J_{sc} . This result is surprising considering that the current collecting CdTe/CdS junction is farther away in this case. Specifically, the CdTe layer is ~ 1.2 μm thicker for devices finished with CBD CdS because these samples only passed through the VTD reactor once (*vide supra*). SEM revealed significant height variations in the deposited CdTe, and the higher J_{sc} can be attributed to a more conformal CdS layer produced by CBD (see Supplementary Information). For completeness, we note that the VTD CdS devices displayed higher efficiencies in comparison to the CBD CdS devices when illuminated through the front of the device despite the fact that the CdS layer was significantly thicker.

A most surprising result from the backside illumination studies is the lack of rollover in the J-V characteristics. Since the polarity of the photovoltage and the direction of the photocurrent is the same for frontside and backside illumination, the electric field must be in the same direction throughout the device. Consequently, we can conclude that the dopant density is indeed low, in agreement with the band diagram of Figure 2a rather than that of Figure 2b. Because photoexcited carriers rapidly relax to the band edges of the CdTe semiconductor, holes should be transported to the back contact at approximately the same electric potential regardless of whether the illumination was from the front or back of the device. This view assumes that the intensity or wavelength distribution of the light does not affect the band edge positions or the transport properties at the back contact. However, J-V results for frontside illuminated devices clearly show the effects of a barrier to hole transport at the back

contact (Fig. 1a), while there is no evidence for such a barrier when the device is illuminated through the back (Fig. 3a and Supplementary Information Fig. S5).

Figure 3b shows the backside internal quantum efficiency that was obtained by normalizing the measured EQE data to the transmission spectrum of the TEC 15M/25 nm SWCNT stack. The carrier collection efficiency for the device with 200 nm of VTD CdS is negligible at the short wavelengths, rises gradually to ~10% near 800 nm, and peaks at >40% at ~830 nm. The peak in carrier collection efficiency for the longer wavelength, above-gap photons is consistent with light absorption and carrier generation deeper in the CdTe and closer to the CdTe/CdS junction. In contrast, the response of the device with 100 nm of CBD CdS rises quickly with increasing wavelength to ~40-50% at 400 nm and remains relatively high until a peak of ~70% is reached at ~830 nm. Once again, the peak in the response at the longer wavelengths is consistent with more efficient collection of carriers generated near the CdTe/CdS junction, but the flat and relatively high collection efficiency across the shorter wavelengths is striking in comparison to the data for the VTD CdS device. The higher J_{sc} in the devices with CBD CdS is evidently due to more efficient collection of carriers generated far from the junction. Surprisingly, the collection efficiency is reasonably high even for 400 nm photons, 95% of which would be absorbed within 100 nm of the SWCNT contact. Note that the electric field is not expected to be strong in this region of the device for a CdTe doping density of $1 \times 10^{12} \text{ cm}^{-3}$ (Fig. 2a), so the high collection efficiency is not expected for carriers generated so close to the back contact. Though speculative, the behavior is suggestive of a lower back surface recombination velocity for minority carriers in the case of the CBD CdS samples, and/or a significantly longer minority carrier diffusion length. The underlying reasons for the differences in behavior for the devices with CBD and VTD CdS are not clear at this time. One possibility is that the second pass through the VTD reactor may have degraded the quality of the CdTe layer through a high temperature materials reaction with the TEC 15M substrate or the SWCNT layer. More study is required to discriminate among the possibilities, but it is clear that devices finished with CBD CdS are more efficient than those finished

with VTD CdS when illuminated through the back contact, while the reverse is true for illumination through the front contact.

To gain further information, frontside and backside J-V data were obtained as a function of light intensity. Figure 4 shows that the characteristic rollover persists across the range of intensities for frontside illumination, while no rollover is observed for illumination through the back contact. It is interesting to note that the slope of the J-V curves in forward bias are strongly dependent on the light intensity in a manner that is consistent with the photogenerated carrier density being comparable to the doping level. This can be seen most clearly in the backside illumination data where the rollover is not evident. One can speculate that the elimination of the rollover behavior with backside illumination could be associated with the larger amount of light absorbed in the SWCNT layer. Only photons with energy less than the band gap energy of CdTe would be incident on the SWCNT layer with frontside illumination, and only a fraction of these would be able to photoexcite carriers across the bandgaps of the s-SWCNTs in the sample. In contrast, with illumination through the back contact the SWCNT layer would be exposed to nearly the full simulated AM1.5 spectrum, including photons with energies above the band gap of CdTe. Photoexcitation across the SWCNT bandgaps would lead to the generation of free carriers [30] that could screen the potential barrier and assist in mediating recombination of electron from the TEC 15M and holes from the CdTe at the back contact.

To further investigate this possibility, the PV performance of several devices was compared while illumination was directed through the front, back, and both contacts simultaneously. The illumination through the ZnO front contact was the AM1.5 spectrum from the solar simulator, while the illumination directed at the back of the device was a fraction of the off-normal output of the simulator that was redirected by reflection using a mirror. The two light beams could be independently blocked without moving the sample. Figure 5 shows representative data from a CBD CdS device. When the device was illuminated through only the front contact, the rollover behavior was observed. Once again, no rollover was observed with only backside illumination. Interestingly, the rollover in

the forward bias current was also not observed when both illumination sources were employed. At 22.3 mA/cm^2 , the J_{SC} when both sides were illuminated was greater than the sum of the J_{SC} values measured for only frontside (17.8 mA/cm^2) and only backside (2.8 mA/cm^2) illumination. The efficiencies were also not additive, and the efficiency obtained for this particular device by combined illumination (5.9%) was enhanced by 11% over expectations based on a linear combination of the frontside (4.6%) and backside (0.7%) illumination for this particular device. The data in Figure 5 shows that the origin of the enhancement in the efficiency is due to a lower series resistance and, consequently, a higher Fill Factor. Apparently, a relatively small amount of backside illumination is able to reduce the back contact barrier and boost the overall efficiency of the device. This result is consistent with the idea that the SWCNT layer mediates the recombination of electrons from the TEC 15M and holes from the CdTe, with the recombination being enhanced by carrier generated by illumination of the SWCNT layer. Turning to the band diagram of Fig. 2a, we can consider that electrons excited within the SWCNT could equilibrate with majority electrons in the n-SnO₂ layer of the TEC 15M by tunneling through the thinner i-SnO₂ layer. The net result would be a smoothing of the potential barrier for electrons to enter the SWCNT from the TEC 15M. Since it is energetically downhill for holes to enter the SWCNT layer from the p-type CdTe, recombination between electron and holes could then proceed at high rate.

Because the SWCNT layer is able to serve as a buffer layer between the n-type TEC 15M TCO coating and the p-type CdTe, the rollover behavior associated with the n/p back contact can be reduced, particularly under backside illumination, to achieve higher efficiencies. Consequently, one can imagine application of the SWCNT buffer layer in fabrication of bifacial solar cells for enhanced energy production,[31] partially transparent PV panels for integration into building windows or automobile sunroofs,[32] and in the construction of back-wall solar cells.[33] The results also suggest that SWCNT layers could be employed to form tunnel/recombination contacts for use in thin-film tandem cell structures. High performance p^+/n^+ tunnel contacts that allow monolithic integration of

stacked cells are essential for high efficiency multi-junction cells built in the III-V[34] and amorphous Si/Ge[35] materials systems. In contrast, tandem cells built from materials such as CdTe, CuInSe₂, or related materials, are difficult to fabricate due to the lack of good tunnel junction contacts and restrictions on device configurations.[36] The potential to facilitate interconnection between cells formed from dissimilar materials with SWCNT layers is enticing, and will be the subject of future work.

4. Conclusions

We fabricated CdTe/CdS solar cells in the substrate configuration on thin, transparent SWCNT back contacts, without the use of copper, and used the VTD manufacturing process to grow the CdTe and CdS layers. A best device efficiency of 6.5% was measured for illumination through the front ZnO contact even though the device efficiency was limited by a thick CdS window layer and current blocking in the TEC 15M/SWCNT/CdTe stack at the back contact. We determined that the rollover behavior normally associated with the poor back contact could be eliminated with backside illumination of the SWCNT layer. Comparison of the J-V and QE data from backside and frontside illumination indicated that the SWCNT layer acts as a recombination/tunnel contact that may be of use in bifacial and a tandem PV device structures.

Appendix A. Supplementary Information

Supplementary information related to this article includes J-V measurements of the superstrate device, SEM images of the CdTe and CdS surfaces before and after CdCl₂ treatment, device area calculation, and advanced J-V analysis of devices illuminated through the backside.

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Table 1: Device data for solar cells prepared in the substrate configuration on a SWCNT back contact interface layer under simulated AM1.5 solar irradiation. Fifteen cells were measured to calculate average values and standard deviations. The stated error in Jsc includes the uncertainties in both the device area and current measurements. Data from the highest efficiency device is also shown.

Voc (mV)	Jsc (mA/cm ²)	FF (%)	Efficiency (%)
666 ± 16	17.4 ± 1.1	49.4 ± 2.0	5.8 ± 0.8
691	18.6	50.4	6.5

Figure 1. (a) Current density-voltage (J-V) curve for the best 3.3 μm CdTe/200 nm CdS device deposited by VTD on TEC 15M substrates with an intervening 25 nm thick SWCNT back contact interface layer. Also shown is a J-V curve from a device that was deposited directly on TEC 15M (no SWCNT layer). (b) Representative external quantum efficiency data for a device with a SWCNT back interface layer.

Figure 2. Band diagrams for TEC 15M/SWCNT (25 nm)/CdTe (4.3 μ m)/ CdS (200 nm)/IZO (80 nm)/AZO (800 nm) devices generated using SCAPS modeling. CdTe doping density was (a) $1 \times 10^{12} \text{ cm}^{-3}$ and (b) $5 \times 10^{14} \text{ cm}^{-3}$.

(a)

(b)

Figure 3. Backside illuminated (a) J-V and (b) Internal quantum efficiency data for representative 3.3 μm CdTe/200 nm CdS (VTD) and 4.3 μm CdTe/100 nm CdS (CBD) devices. Also shown in (b) is the transmission spectrum for a 25 nm SWCNT film on TEC 15M, normalized to 100% at ~600 nm. The actual transmission of the TEC 15M/25 nm SWCNT stack is ~64% at 600 nm.

Figure 4. J-V measurements as a function of light intensity for a 4.3 μm CdTe/100 nm CdS (CBD) device illuminated through (a) the frontside and (b) the backside of the device.

Figure 5. J-V response of 4.3 μm CdTe/ 100 nm CdS (CBD) device illuminated through the front, back, and both sides of the device.