Embedded Nanowire Window Layers for Enhanced Quantum Efficiency in Window-Absorber Type Solar Cells like CdS/CdTe

Hongmei Dang, Vijay P. Singh, Sai Guduru, and Jeffery T. Hastings*

Department of Electrical and Computer Engineering, and Center for Nanoscale Science and Engineering (CeNSE), University of Kentucky, Lexington, KY, 40506-0046, U.S.A.

E-mail: vsingh@uky.edu

Abstract

Embedded CdS nanowires are used for improving the spectral transmission of the CdS window layer, thus enhancing the quantum efficiency of CdS-CdTe solar cells. Substantially higher light transmission is observed in the 300nm-550nm wavelength range. A nearly ideal spectral response of quantum efficiency over a wide spectral range provides evidence for improved light transmission through the window layer and enhanced absorption and carrier generation in the CdTe absorber layer. Nanowire CdS/CdTe solar cells on SnO₂/ITO-soda lime glass substrates, and with Cu/graphite paste/silver paste as back contact electrodes, yield a power conversion efficiency of 12%. MoO_{3-x}/Au back contacts were also investigated. With these back contacts, the nanowire CdS-CdTe solar cells exhibit efficiency comparable to the efficiency of their planar CdS counterparts. Junction transport mechanisms are delineated for advancing the basic understanding of device physics at the interface. Our results prove the efficacy of this nanowire approach for enhancing the quantum efficiency in window-absorber type solar cells (CdS-CdTe, CdS-CIGS and CdS-CZTSSe etc.) and other optoelectronic devices.

KEYWORDS CdS Nanowire Window Layer; Nanowire CdS-CdTe Solar Cells; Light Transmission; Quantum Efficiency

1. Introduction

Third-generation photovoltaic technologies develop nanostructured devices and materials as a general approach to create beneficial optical management, novel conversion mechanisms and improved carrier collection efficiency [1-3]. Nanostructures have been used extensively in polymer-based [1, 4-6], dye-sensitized [7-10] and silicon solar cells [3, 11, 12] for effective light absorption and carrier collection. Their advantages have rarely been applied to the window-absorber type solar cells, including the devices using CdS window layer coupled with an absorber layer of CdTe, CIGS, or the earth-abundant-CZTSSe, which are the most cost-effective photovoltaic technologies and are potentially competitive with conventional power sources for terrestrial applications [13-16].

The CdS-CdTe solar cell is a window-absorber type device structure, where CdS is approximately 50-100nm thick and functions as a window layer. CdTe is approximately 6-8 μ m thick, has crystallites of relatively large size, and functions as an absorber material of close to ideal energy band gap (Figure 1A). One of the issues that limit efficiency in this cell is the loss of photocurrent due to significant light absorption in the traditional planar CdS window layer.

Planar CdS is responsible for parasitic light absorption loss of 22-24% and a photocurrent loss of approximately 7 mA/cm² [14,17,18]. A planar window layer thinning method [14] and a method of widening band gap of the CdS window layer by Cd_{1-x}Zn_xS alloy [19] created moderate gain in transmission; however they present significant challenges in substrate roughness and pinholes. Issues. . In addition, due to polycrystalline CdS with pinholes and high defects, planar CdS can accelerate cell degradation because Cu, usually included in back contacts, diffuses farther into SnO₂ through pinholes and defects of the planar CdS, forming deep penetration and introducing micro-shunts [20]. As a result, main junction and the conductive back contact behaviour are aggravated [20].

In this paper, we present an approach for overcoming these challenges through a stack nanowire solar cell structure with diffused p-n junction. The stack nanowire solar cell configuration is an array

of CdS nanowires embedded in a transparent anodized aluminum oxide (AAO) matrix which replaces planar CdS as a nanowire window layer for tailoring optical properties, a CdTe absorber layer grown on the top of them; this nanowire CdS-CdTe device structure is illustrated in Figure. 1B; note that it is substantially different from the CdS nanopillar structure described in [21]. Carrier generation and transport of the stack nanowire and the conventional planar CdS-CdTe solar cells are shown in Figure 1C and 1D. The fine features of the CdS nanowires confined by nanopores in AAO matrix favourably increase the optical energy band gap and extend transmittance edge of CdS [22-24]. Under such circumstances, a part of incident light across the entire spectrum range can directly transmit through absorption-negligible AAO matrix (Figure 1C), and the other part of incident light transmitted through CdS nanowires (Figure 1C) can be enhanced due to their larger effective energy band gap [22-24].

Even for photons of long wavelengths, whose energy is smaller than the band gap of CdS, the transmission of thin film CdS is less than 100%; there are still finite optical losses. These losses in the long wavelength range are expected to be smaller when 68% of the CdS film is replaced by the anodized aluminium oxide (AAO) matrix, which holds the CdS nanowires in the device design investigated in this paper. But, in practice, there are other effects, like increased scatter from the nanowire geometry, which counter this advantage. Further investigations into these effects are underway in our laboratory.

Hence, much broader and stronger spectral range of incident light reaches the CdTe absorber layer where photons are absorbed and converted to carriers. Such configuration significantly suppresses parasitic absorption loss in the window layer, and extends the optical generation of carriers into the broad solar spectrum, resulting in enhanced light absorption and carrier generation and collection. In the following sections, transmission gain in the nanowire window layer, an ideal and wide quantum efficiency response for improved light absorption and carrier collection, power conversion efficiency and a charge transport model and defect analysis are presented.

Figure 1. (A), Schematic structure of a planar CdS/CdTe solar cell. (B), Schematic structure of a vertical stack nanowire CdS/CdTe solar cell, where light colour represents absorption- negligible AAO. (C), Electron and hole transport through reduced junction interface area in the nanowire CdS/CdTe solar cell. (D), for comparison, electron and hole transport through junction interface in a conventional planar CdS/CdTe solar cell, figure 1C and 1D are schematic, where the number of electrons in planar CdS is the same as the number of the CdS nanowires.

2. Experimental Procedures

Figure2 illustrates the major processing steps in the fabrication of a nanowire CdS/CdTe solar cell.

Figure2. Major processing steps in the fabrication of a nanowire CdS/CdTe solar cell

AAO membrane fabrication and CdS nanowire growth: Commercially available ITO/ soda-lime glass substrates with sheet resistance of 23-28 Ω /square were cut into 1 inch by 1 inch pieces and cleaned in acetone, methanol, and de-ionized water and dried in nitrogen flow. A 100 nm thick tin oxide (intrinsic SnO_2) layer and a 5 nm thick titanium layer were deposited on ITO by r.f. sputtering. Next, a 100 nm thick layer of aluminum metal was deposited by electron beam evaporation. Anodized aluminum oxide (AAO) membranes were formed by the following steps. The Al/ Ti/ SnO_2 /ITO glass substrates were anodized in a 0.3 M oxalic acid solution under a 50 V bias until Al was completely anodized. Anodization consists of two competing chemical processes, which are set off by the flow of current through the electrolyte and the aluminium film. These are, (i) oxidation of the 100 nm thick aluminium layer resulting in the formation of aluminium oxide and, (ii) consumption of aluminium oxide by

dissolution into the electrolyte solution. These two competing processes result in the formation of nanopores inside the aluminium oxide layer, making it look like a membrane. These pores are uniformly distributed and have diameters in the range of 10-100 nm; the actual value of the pore diameter is controlled by a host of process parameters like the chemical composition of electrolyte, and the current across the electrolyte and the aluminium layer etc. At the conclusion of the anodization process, pores go right through the original aluminium-titanium films, but a very thin layer of aluminium oxide- titanium oxide is left at the bottom of each pore; this is called the “residual layer”, or the “barrier layer”. This layer is only about 2-10 nm thick, and many times is not even continuous. Still it must be removed, to ensure that, later, electrochemical filling of the pores with CdS nanowires, can proceed in a complete and uniform filling of all the pores in the AAO host. Such removal of the residual layer is accomplished, in practice, by special etching processes involving phosphoric acid and reactive ion etching (RIE) etc.

Next, samples were etched in 5% phosphoric acid for 40 minutes at room temperature to partially remove the barrier layer. This was followed by a reactive ion etch (RIE) process for 2 min to completely remove the barrier layer; RF and ICP power values were set at 90W and 250W respectively during the RIE process. Then, the samples were etched in 5% phosphoric acid for 5 minutes and rinsed by deionized water, resulting in formation of AAO membranes on transparent SnO₂/ITO glass substrates.

Electrolyte for the CdS nanowires deposition is a mixture of 0.055M cadmium chloride (CdCl₂) and 0.19M elemental sulphur in 50mL dimethyl-sulfoxide (DMSO) solution. The CdS nanowires were formed at the deposition temperature of 160°C, and under a dc current density of 7mA/cm², based on the total area of the sample. In fact the CdS gets deposited only in the pores of the AAO membrane. These pores occupy 32% of the total surface area. Therefore, based on the actual area of nanopores within the alumina layer, the current density is 21.88 mA/cm². Following growth, the CdS nanowires

were soaked in a 75%-saturated CdCl_2 in methanol solution for 15 minutes. After the soak, the CdS nanowires were annealed at 400°C for 30 minutes with 100-sccm Argon flow.

Fabrication of CdTe absorber layer and back contact: Next, p-CdTe absorber layer was deposited in a closed-space sublimation system in a 2-step process,

- (i) In the first step, CdTe powder (99.99% Alfa Aesar) acted as the “source”. It was heated to 625°C to deposit a 30 micrometer thick CdTe film on a molybdenum substrate. This took 20 minutes, and during that time, the temperature of molybdenum substrate was held at 525°C ; spacing between the source and substrate was 2 mm.
- (ii) In the second step, CdTe coated molybdenum substrate acted as the “new source” and the (nanowire CdS/i-SnO₂/ITO/glass) sample acted as the “substrate”. During the deposition of CdTe films on the samples, the chamber was pumped down to a background pressure of approximately 0.35 torr; then He with 5% O₂ was introduced at a total pressure of 15 torr. The source and substrate were ramped together to 570°C , and then the source temperature was quickly increased to 630°C . The source and substrate were maintained at 570°C , and 630°C for 2.3 minute deposition; again, the source-substrate distance was 2mm.

After the deposition of the p-CdTe absorber film, CdCl_2 annealing treatment was performed. The samples were soaked in a 75% CdCl_2 in methanol solution for 20 minutes, and then placed in an annealing furnace at 400°C for 30 minutes with a 100-sccm flow of Argon.

Before the deposition of contact electrode to CdTe, the cells were etched in a solution of nitric and phosphoric acid (1% HNO_3 , 88% H_3PO_4 , and 35% DI-water) for 35seconds. This purpose was to clean up the surface of CdTe film and render it tellurium rich (Te^+). The cells were then masked to define the back contact area. Next, 5 nm thick copper layer was deposited onto the back contact area by sputtering. Graphite paste (with 1200-2400 $\Omega/\text{sq.}$) and silver paste electrodes were painted on to the

back contact area. The cells were then heated at 150 °C for 10 min to facilitate forming a Cu₂Te layer and for curing the graphite/silver paste electrode. To separate solar cell dots and to define the area of each cell, a cutter tool was used to cut through the p-CdTe and CdS layer. The area of a typical such cut/scratch, as measured under an optical microscope, was 0.018mm²; this was also the area of record for that device.

For MoO_{3-x}/Au back contact, without NP etch, MoO₃ thin films with a thickness of 10 nm were thermally evaporated on clean CdTe surfaces from stoichiometric MoO₃ powder (Alfa Aesar, 99.9%), where the pressure was less than 1*10⁻⁵ Torr and the deposition rate was maintained as 0.5 Å/s. Before the vacuum evaporation of MoO_{3-x} buffer layer on top of CdTe surface, parts of CdTe samples were masked by Aluminum foils. This was done to define the outer limits of patches within which the Au electrodes would be, later, sputter deposited. After MoO_{3-x} deposition, the samples were annealed at 200°C in N₂ for 10 minutes.

Next, 15nm thick Au electrode dots were sputter deposited within the MoO_{3-x} patches. After depositing Au layer, all samples were annealed at 200°C in Argon for 10 minutes. The devices were then scribed around the Au electrode to define the solar cell area for the purpose of materials and electro-optical characterizations of these NW-CdS/CdTe solar cells with MoO_{3-x} p-Au electrodes”.

Materials and device characterization: Material characterization of the CdS nanowires was conducted with a scanning electron microscope (Hitachi S-900 field emission SEM). Optical transmittance spectra were measured with a Cary, Model 50 Probe UV-Visible Spectrophotometer. Current–voltage (*I* –*V*) characteristics were measured using a solar simulator, Science Tech SS 150, whose radiation intensity was set at 100 mW/cm². Quantum efficiency data was extracted from measurements made by an independent photovoltaic measurements company, called PV Measurements Inc., of Colorado, U.S.A. Electrical properties of the nanowire CdS-CdTe solar cells were characterized by current–voltage (*I*–*V*) and capacitance-voltage (*C*-*V*) measurements as functions of

light intensity and temperature in the 175 °K -300 °K range. For temperature variation, nanowire solar cells were mounted inside an Oxford's vacuum cryostat with a helium refrigerator unit (Sumitomo Heavy Industries Ltd). A standard Science Tech SS150 solar simulator was used for device illumination; it simulates the AM 1.5 spectrum. C-V characteristics were measured with an Agilent 4284A capacitance meter at a frequency of 1MHz. Capacitance-frequency measurements at zero bias were also measured with this instrument over the frequency range of 1 KHz to 1 MHz.

For obtaining approximate values of device parameters, the “total” intensity of light incident on our solar cell devices was set at 100 mW/cm² with the help of a power meter. However, exhaustive device calibration including spectrum matching and/or sending the device to an international calibration laboratory, was not done. Also, the device area was defined by scribing around the top electrode, deep through the CdTe and CdS films, and then measuring by viewing under an optical microscope. Still, the area is small, and measurement could be off, easily by 5% or more. Therefore, the values of short-circuit current, power conversion efficiency etc., reported in this paper, can be off by as much as 10%.

3. Results and Discussion

3.1 SEM Characterization

To realize the above advantages offered by nanowire window layer solar cells, there is need for a relatively inexpensive process to economically fabricate large periodic arrays of semiconductor nanowires. To this purpose, we developed a lost-cost, template-assisted and metal catalysts-free electro-deposition process, to simply and efficiently grow 100 nm-CdS nanowires on transparent substrates (see Supplement Materials in Experimental section). The key points are that due to fine geometric confinement of the AAO membrane, the CdS nanowires maintain their nanostructure characteristics during the various subsequent high temperature processes. Figures 3A and 3B show the top views of scanning electron microscopy (SEM) images of the nanoporous AAO membrane and the

free-standing CdS nanowires, respectively, and figure 3C shows the cross-sectional view of CdS nanowires embedded in the AAO matrix. Free standing CdS nanowires shown in Fig. 3B were obtained by removing the embedding AAO membrane with a chemical etch in the 1N NaOH solution. Due to its highly selective etching property, the NaOH solution removed the embedding AAO, but did not react with cadmium sulfide nanowires.

A fracture/crack can be seen in Figure 3C of the original manuscript. On the right side of fracture, more nanopores of AAO membrane are filled with CdS nanowires than on the left of the fracture. To get a good cross sectional view in the SEM, the sample needs to be fractured; this requires a strong mechanical blow, which often causes the CdS nanopillars to fall out of their embedding pores because of very high mechanical stress. Figure 3B shows the top view and that SEM sample was not subjected to hard mechanical blow. From Figure 3B, it can be inferred that pretty much, all pores have CdS nanowires embedded in them.

From figure 3C, it is seen that CdS nanowires are highly ordered, vertically aligned and dense. Length, diameter and the average distance between the centres of neighbouring nanowires were estimated at approximately 100 nm, 60 nm and 106 nm respectively. The porosity of the AAO membrane and the area density of CdS nanowires were calculated to be 32% and 1.14×10^{10} nanowires/cm² respectively. Such well-aligned nanowire arrays produced from the quasi-periodic arrangement of transparent AAO membranes are advantageous because they exhibit lower optical reflection than the arrays of random arrangements [3,25,26]. It should be noted that different forms-fully embedded and free standing nanowires can be readily grown, and various nanowire parameters including length, diameter and pitch could be varied controllably (see Experimental section). By changing the AAO membrane processing parameters, the diameter and length of CdS nanowires could be varied controllably over the relatively wide ranges of (10-100) nm and (100-6000) nm respectively. As an example, diameter could be reduced by decreasing the applied voltage during the anodization

process; and the length could be increased by simply increasing the thickness of aluminum layer deposited on the substrate before the formation of AAO membrane by anodization.

Furthermore, the AAO membranes and the nanowires can be grown on a large variety of rigid and flexible substrates, indeed all substrates, which allow for the deposition of aluminum (Al) film and its anodization.

Figure 3. SEM images; (A), top view of a nanoporous membrane of anodized aluminium oxide (AAO); (B), top view of an array of 100 nm long free-standing CdS nanowires; (C), cross-sectional view of a 100 nm long CdS nanowire array embedded in the AAO membrane.

3.2 Spectral Transmittance of CdS Nanowire Window Layer

For gaining a quantitative understanding of the transmission advantage of the 100 nm long, embedded CdS nanowires layer over the 100 nm thick, traditional planar CdS film; we compared the spectral transmission of both in the wavelength range of 300-860 nm (Figure 4A). The substrate in both cases was a 100 nm thick tin oxide (SnO_2) layer sputtered on top of the ITO-coated-soda lime glass. The transmission spectrum of the 100nm thick AAO membrane (Figure 4B) exhibits practically complete transmission at wavelengths longer than 240nm. It is clear that absorption-negligible characteristics displayed by AAO membranes make them an ideal choice for the development of nanostructure designs for a host of applications in solar cells and other optoelectronic devices.

At wavelengths longer than 550 nm, where the photon energy is smaller than 2.4 eV (the energy band gap of planar CdS), the two curves overlap each other. However, the CdS nanowire curve shows substantially higher transmission from 335 nm to 550 nm, while in this wavelength range, the spectral transmission of planar CdS is very poor. This difference could arise from, (i) the larger effective energy band gap of the nanowire CdS layer leading to higher optical transmission than that of the planar CdS layer[22-24] and/or, (ii) the nanowire CdS covering only a fraction (32%) of the substrate, the rest covered by the embedding AAO matrix.

In the long wavelength range, for example at 860 nm, the transmission of the CdS- SnO_2 -ITO-soda lime glass stack is about 70%. Thus, substantial optical losses are due to the intrinsic- SnO_2 /ITO/the soda-lime glass. Higher transmission can be obtained by replacing the intrinsic- SnO_2 / ITO/the soda-lime glass with a higher transmission, higher quality substrate[14]. On the other hand, the higher transmission glass is more expensive and would add to the manufacturing costs.

Note that even for photons of long wavelengths, whose energy is smaller than the band gap of CdS, the transmission of thin film CdS is less than 100%; there are still finite optical losses. These losses in the long wavelength range are expected to be smaller when 68% of the CdS film is replaced by the

anodized aluminium oxide (AAO) matrix, which holds the CdS nanowires in the device design investigated in this paper. But, in practice, there are other effects, like increased scatter from the nanowire geometry, which counter this advantage. Further investigations into these effects are underway in our laboratory.

It is clear that the CdS nanowires as the novel window layer suppresses the absorption loss at wavelengths below 550 nm and the spectral range of photons reaching the CdTe absorber is dramatically increased to 300-860 nm, compared to the 512 -860 nm range for the case of the planar CdS counterpart. . Because of the fact that the photons are absorbed and converted to the photocurrent in the absorber layer, the two effects lead to enhanced carrier conversion for the nanowire solar cell configuration.

To gauge the effect of the transmission enhancement advantage of the CdS nanowires on the photocurrent (S_C) of the nanowire solar cells, the overall photon flux (P) reaching the CdTe absorber was calculated. Figure 4C shows the photon flux $P_{\text{nanowires}}$ that can be converted to the photocurrent in the nanowire solar cells, and also shows the photon flux P_{planar} in the planar solar cells for comparison. The nanowire solar cells yield the photon flux which is higher than that of its planar counterpart in the wavelength range of 300 nm to 550 nm. The additional photon flux reaching the CdTe absorber layer because of the enhanced transmission of CdS nanowires window layer is plotted as a function of wavelength in Figure 4D.

Figure 4. Transmission spectra of, (A), the 100 nm long embedded CdS nanowires and of 100 nm thick planar CdS film on the intrinsic-SnO₂/ITO/the soda-lime glass substrate; (B), 100 nm thick AAO membrane; (C) the intrinsic-SnO₂/ITO/the soda-lime glass; (D), Photon enhancement in the CdS nanowire solar cells; in all cases, the substrates is SnO₂/ITO/Soda-lime glass.

The photon flux data of Figure 3 indicates that a solar cell employing a CdS nanowire window layer would yield a higher S_C value than the cell with a planar CdS window layer. It is estimated that the total number of carriers and J_{sc} are $18.65 \times 10^{16}/\text{cm}^2\text{s}$ and $29.84 \text{ mA}/\text{cm}^2$ for the nanowire solar cells. These numbers exceed the corresponding values of $15.64 \times 10^{16}/\text{cm}^2\text{s}$ and $25.03 \text{ mA}/\text{cm}^2$ for the planar

counterpart. The J_{sc} increases by 4.81 mA/cm^2 , which corresponds to a gain of 19.2% when the CdS nanowires window layer replaces the planar CdS window layer. In a hypothetical case where transmittance of a substrate is approximate 100%, J_{sc} values for the nanowire solar cells and counterpart planar solar cells were calculated to be 32.1 mA/cm^2 and 26.6 mA/cm^2 respectively, constituting an increase of 5.49 mA/cm^2 in J_{sc} and a gain of 20.6% over the base. Hence, one can expect even higher J_{sc} values in the future, when intrinsic SnO_2/ITO -soda lime glass substrates in the present device configuration are replaced by high quality transparent substrates.

Another advantage of the nanowire solar cells is that because CdS nanowires embedded in AAO membrane typically take up only about 32% of the physical area, the interface area at the junction between CdS nanowires and CdTe is reduced approximately by a factor of 3. When interface recombination is the dominant electron transport mechanism across the heterojunction, which appears to be the case for these CdS-CdTe solar cells, then reduction in interface area may lead to an equivalent reduction in the effective reverse saturation current I_0 provided that the AAO/CdTe interface does not introduce a recombination problem affecting the effective carrier lifetime. Since the open circuit voltage V_{oc} is dependent on I_0 and short current I_{sc} , both of these effects may result in gain of approximately 7.3% in V_{oc} provided that the AAO/CdTe interface does not introduce a recombination problem. Overall, the J_{sc} gain of 19.2% and the V_{oc} gain of 7.3% may lead to a cumulative gain of 27.8% in the power conversion efficiency of the CdTe solar cell on intrinsic SnO_2/ITO -soda lime glass substrates. The corresponding gain in the power conversion efficiency of the CdTe solar cell on high quality transparent substrates may be 30%.

3.3 Quantum Efficiency of Nanowire CdS-CdTe Solar Cells

Figure 5A shows the normalized spectral response of the external quantum efficiency (EQE) of the (intrinsic soda-lime glass/ITO/ intrinsic $\text{SnO}_2/\text{NW-CdS/CdTe}$ /graphite paste) solar cell device,

which was measured by an independent group at the PV Measurements Inc. EQE value increases steadily from 40% at 335 nm to 80% at 380 nm, and 90% at 450 nm; it peaks at 535 nm, and then stays practically constant until reaching the energy band gap edge of the CdTe absorber layer. In the 300 nm to 550 nm wavelength range, the EQE response of the nanowire solar cells, shown in Figure 4a, is substantially higher than reported by other groups who have tried to enhance the quantum efficiency of CdS-CdTe solar cells by various other methods, which include reducing the thickness of the planar CdS window layer and increasing the optical energy band gap by alloying[13-16, 19, 27-33]. Such strong EQE response at very wide spectral range proves that the CdS-CdTe solar cells including CdS nanowires as the window layer enhance light absorption and carrier generation and collection. It should be noted that the above device is built on the inexpensive and low transparent intrinsic SnO₂/ITO/soda lime glass substrate. Later, when such low transparent substrate is replaced by a higher transmission substrate, the EQE response of the nanowire window-absorber solar cells will be even further improved.

Wu et al used nanocrystalline CdS:O of 70-80 nm thickness for the window layer[14]. However EQE enhancement in their device was much smaller than seen in Figure 5A. In their case[14], EQE reached 90% of its maximum value at approximately 500 nm, while for our device, EQE reaches 90% at approximately 450 nm. One possible reason is that our embedded CdS nanowires can maintain their fine nanostructured features even when exposed to subsequent high temperature CdTe deposition and CdCl₂ annealing treatments. On the other hand, Wu et al's nanocrystalline CdS film (nano-CdS: O) can lose its nanocrystalline structure feature due to the grain growth and recrystallization that happen during the high temperature treatments. However, the latest high efficiency CdTe cells have achieved better transmission through the planar window layer and have spectral responses similar to the spectral responses of the nanowire CdS-CdTe solar cells [34, 35].

Energy band gap widening in CdS by alloying is another approach that has been investigated [19] with success, because higher transmission was achieved and the spectral range was widened, down to 300 nm in wavelength. However, their approach to transmission enhancement requires the availability of a suitable alloy, while the embedded nanowire approach presented in this paper is, in theory, more universally applicable to window-absorber type optoelectronic devices.” Of course, in general, the two approaches can supplement each other.”

Also, comparing the EQE response of Figure 5A in the (300-550) nm range with those of the CdS-CIGS [15, 27-29, 33] and CdS-CZTS cells [16, 30-32, 36] employing thin CdS layers, it becomes clear that the nanowire CdS approach is substantially superior to the “thinning CdS” approach, and performance of CdS-CIGS and CdS-CZTS cells would also be further improved if nanowire CdS were to be used as a window layer in that technology.

Figure 5: (A), EQE of the nanowire CdS/CdTe solar cells without antireflection coating; (B), J-V characteristics of the nanowire CdS/CdTe/Cu/graphite/Silver paste solar cells, without antireflection coating under dark and 1-sun illumination. (C) J-V characteristics of the nanowire CdS/CdTe/MoO_{3-x}/Au solar cells, without antireflection coating under dark and 1-sun illumination.

3.4 J-V Characteristics of Nanowire CdS/CdTe Solar Cells

Figure 5B shows the J-V characteristics of one of our best nanowire CdS/CdTe solar cells, when tested under standard conditions of room temperature and 100 mW/cm² irradiation. The cell had an area of 0.018 cm², and yielded an open-circuit voltage V_{oc} of 770 mV, a short current density J_{sc} of 26 mA/cm², a fill factor, FF of 60%, and a power conversion efficiency (PCE) of 12%. After integrating the data of Figure 5A with the spectral output of the Science Tech Solar Simulator (AM 1.5), the light generated current density of our solar cell was calculated to be 25.9 mA/sq.cm., with a 10% error margin; this is close to the experimentally observed short-circuit current density value of 26 mA/sq.cm., also with a 10% error margin. In these experimental and calculated values of current densities, error margins arise from uncertainties in power supply voltage output, stability of light sources and the determination of the solar cell device area etc.

It should be noted that the 12% efficiency value was achieved in our laboratory on an intrinsic SnO₂/ITO-soda-lime glass substrate and without antireflective coating. This is the first time that a nanowire CdS/CdTe solar cell has displayed an efficiency value higher than 10%.

The relatively high value of 26 mA/cm² for J_{sc} in the stack nanowire CdS-CdTe solar cell is significantly higher than J_{sc} of 21 mA/cm² in core-shell nanopillar CdS-CdTe solar cells [21]. Higher J_{sc} is attributed to the stack, diffused p-n nanowire solar cell configuration for transmission gain in the nanowire window layer and light absorption gain in the CdTe absorber. It is higher than the J_{sc} of 25.88 mA/cm² reported in their high efficiency thin film CdS/CdTe solar cell, which employed a planar CdS with 70-80nm thickness for the window layer [14]. However, their solar cell device had two other extraneous advantages, (i) an antireflection coating and, (ii) a high quality, high cost CTO/ZTO/Corning 7059 glass substrate instead of the low cost, commercial, intrinsic SnO₂/ITO/soda lime glass substrate used in our device.

As of now, the 770 mV value for the V_{oc} of the nanowire solar cell device structure is notably higher than V_{oc} of 620mV in core-shell nanopillar CdS-CdTe solar cells [21]. In addition, it is higher than that of other cells (670mV-710mV) based on band gap widening in the window layer[19]. Higher V_{oc} is indeed expected because of the reduced saturation current density due to reduced interface area between CdS nanowires and CdTe as well as the higher photocurrent. Theoretical considerations indicate that these nanowire CdS/CdTe solar cells can achieve V_{oc} of about 925 mV and a resulting increase in PCE of 27.8%-30%. This is illustrated by the following 4 numerical examples. Major assumptions are that, (i) interface recombination current is the dominant CdS-CdTe junction current, and, (ii) CdTe-AAO interface does not degrade the solar cell characteristics.

Consider cell 1 as an example of the planar CdS/CdTe technology; let Voc =850 mV, and J_{sc} =25.03 mA/cm²; Cell 2 represents the corresponding Nanowire-CdS/CdTe device. Then 4 case scenarios are as follows,

CASE I:

- (i) The interface area at the junction between CdS nanowires and CdTe is reduced by a factor of

$$(1/0.32) = 3.125, \text{ as in our experiments. Next, assume, } I_{o1} = 3.125 I_{o2}$$

- (ii) Diode Ideality Factor = $n=A = 2.56$ (measured value for our NW-CdS/CdTe cell in the dark, at room temperature)

- (iii) $I_{L1} = I_{L2}$ (conservative assumption)

$$\text{For planar CdS cell: } V_{OC1} = (nKT/q) \ln (I_{L1}/ I_{O1}) \dots\dots\dots (1)$$

$$\text{For Nanowire CdS Cell: } V_{OC2} = (nKT/q) \ln (I_{L2}/ I_{O2}) \dots\dots\dots (2)$$

$$\text{Therefore, } (V_{OC2} - V_{OC1}) = (nKT/q) \ln [(I_{L2}/ I_{L1}) \times (I_{O1}/ I_{O2})] \dots\dots\dots (3)$$

$$\text{Or, } (V_{OC2} - V_{OC1}) = (2.56 \times 25.9 \text{ mV}) \ln [(1) \times (3.125)] = 75 \text{ mV}$$

Thus open circuit voltage, V_{OC} is enhanced by 75 mV, from 850mV to 925 mV

CASE II:

Same as Case I, except that

- (iv) $I_{L2} = 1.192 \times I_{L1}$ (Current enhancement of 19.2% is expected because of better window layer)

$$\text{Then, } (V_{OC2} - V_{OC1}) = (2.56 \times 25.9 \text{ mV}) \ln [(1.192) \times (3.125)] = 87 \text{ mV}$$

Thus open circuit voltage, V_{OC} , is enhanced by 87 mV, from 850mV to 937 mV

CASE III:

Same as Case I, except that

- (v) Diode Ideality Factor = $n=A = 4.5$ (measured for our NW-CdS/CdTe cell under sunlight illumination, at room temperature)

$$\text{Then, } (V_{OC2} - V_{OC1}) = (4.5 \times 25.9 \text{ mV}) \ln [(1) \times (3.125)] = 133 \text{ mV}$$

Thus open circuit voltage, V_{OC} , is enhanced by 133 mV, from 850mV to 983 mV

CASE IV:

Same as Case III, except that

(vi) $I_{L2} = 1.192 \times I_{L1}$ (Current enhancement of 19.2% is expected because of better window layer)

Then, $(V_{OC2} - V_{OC1}) = (4.5 \times 25.9 \text{ mV}) \ln [(1.192) \times (3.125)] = 153 \text{ mV}$

Thus open circuit voltage, V_{OC} , is enhanced by 133 mV, from 850 mV to 1003 mV

Currently, the V_{oc} of 770 mV in our nanowire CdS/CdTe solar cells is only 84% of the maximum theoretical value. It is thought that the low vacuum (0.35 torr, higher than 0.02 torr used in CdS/CdTe solar cells [37] and low deposition temperature limitations in our current fabrication facilities are responsible for introduction of a large number of defects and traps. The identification of the mechanisms which limit the V_{oc} of the nanowire CdS-CdTe solar cells and the finding of the pathways to further improvements will be discussed in more detail in the following sections.

When $\text{MoO}_3(10\text{nm})/\text{Au}(15\text{nm})$ was used as the back contact to CdTe, the nanowire solar cells yielded V_{oc} of 753 mV, J_{sc} of 25.5 mA/cm^2 , a fill factor, FF of 57.1%, series resistance of $7.72 \Omega/\text{cm}^2$, and a power conversion efficiency of 11%, shown in Figure 5C. This efficiency is still much lower than the highest reported in the literature on planar cells with $\text{MoO}_{3-x}/\text{metal}$ back contacts; those are in the 12.2%-14.1% range [38]-[40]. Substantial improvements need to be made in the series resistance and the fill factor of our devices.

Although our nanowire solar cells, using non-optimal Cu/graphite/silver pastes as back contacts, exhibited efficiency substantially lower than their counterpart best planar CdS-CdTe solar cells reported in the literature[14], efficiency of our nanowire CdS-CdTe cell design with $\text{MoO}_{3-x}/\text{Au}$ back contacts is comparable to efficiency of their planar counterparts [38-40]. We project that the efficiency of the nanowire solar cell can be significantly enhanced in the future through further optimization of CdS nanowire layer and the CdTe absorber layer, avoidance of high resistivity buffer layer of intrinsic

SnO₂, and integration with the several conventional approaches, such as utilizing high conductivity and transparent substrates and applying low resistance back contacts.

3.5 Carrier Concentration Distribution and Interface characteristics in Nanowire CdS/CdTe Solar Cells

Carrier concentration distribution and interface characteristics are critical parameters for identifying the pathways to further enhancement in the performance of nanowire solar cells. They were measured by performing the capacitance-voltage (C-V) measurements, at the fixed, high frequency of 1MHz over a set of temperatures, 300, 275, 250, 225, 200 and 175 °K. The depletion layer width and the net space charge density profile $N(x)$ was calculated. Figure 6A shows the C^{-2} versus voltage characteristics of the nanowire CdS/CdTe solar cell at 300 °K and 250 °K in the dark and under sunlight illumination. These curves are not linear but can be represented approximately by two straight line tangents, one at zero bias and the other at the “strong” bias of -2.5V. Slopes of these two tangents yield the space charge density values, N_1 and N_2 . Table 1 summarizes extracted net space charge density N_1 and N_2 and depletion layer widths at a set of temperatures in the 300 °K to 175 °K range.

From Figure 6A and Table 1, we observe that net space charge density is higher at large reverse bias (-2.5V) than at zero bias. N_1 and N_2 encompass the hole carrier density arising from the shallow acceptor traps near the valance band of the p-type CdTe layer, as well as the “deep” mid gap traps. Depending on the type of impurity or defect, mid gap traps can manifest as donor type trap states or as acceptor type trap states. Reduced value of N_1 in the region nearer to the heterojunction interface in the dark indicates a higher density of donor type traps and/or a lower density of acceptor type traps near the nanowire CdS/CdTe junction [41].

Also, in the dark, both N_1 and N_2 increase as the device temperature is decreased from 300 °K to 175 °K (Table 1). This is understandable because at lower temperature, less energy is available for the

“deep” traps to donate and/or accept an electron; hence their effectiveness is reduced. On the other hand, even at the low temperature of 175 °K, there is enough thermal energy available for the shallow acceptor levels to accept an electron from the valance band of CdTe.

Under one-sun illumination, values of both N_1 and N_2 are smaller than their dark values. This indicates that the active deep mid gap trap in CdTe is the donor type and not the acceptor type. Under illumination, more donor type traps are able to donate electrons to the conduction band of CdTe. This results in additional positive space charge in the midgap traps, which opposes the negative space charge in the shallow acceptor traps. The net value of space charge density (N_1 as well as N_2) is thus reduced.

The shallow acceptor trap level in CdTe is thought to be due to ionized cadmium vacancy, VCd^- acceptor defect and chlorine center $VCd^{2-}-Cl_{Te}^+$ acceptor defect [42]. The deep donor type trap level, on the other hand, may be related to the doubly ionized interstitial Cu^{++} ion [41]. If this is the case for the nanowire CdS/CdTe solar cells, then the inclusion of Cu in the back contact to CdTe may be responsible for this deep trap and the $CdCl_2$ annealing treatment may be partially responsible for the shallow acceptor levels. In addition, the inter-diffusion of sulphur and tellurium across the CdS-CdTe junction is likely to be playing a role as well.

Considering that the deep donor trap is an effective recombination center, further optimization of Cu concentration at the back contact to CdTe and interface passivation to suppress donor trap density will effectively reduce J_0 and enhance V_{oc} for these nanowire CdS/CdTe solar cells. This investigation, including the detailed characterization of mid gap traps is planned in our laboratory in the near future.

Figure 6. (A), C^{-2} versus voltage curves of the nanowire CdS/CdTe solar cell at 300 °K and 250 °K in dark and light; (B), Diode ideality factor (n) and α as functions of temperature in dark and under illumination; (C), Open circuit voltage as a function of temperature under one-sun illumination; (D), Four mechanisms for electron transport across the nanowire CdS-CdTe heterojunction.

Table 1: Depletion Layer Widths and Space Charge Densities of the nanowire CdS/CdTe solar cell at various temperatures.

T(K)	Dark				Light			
	W_0 (μm)	$N_1(W(0))$ $\times 10^{15} \text{cm}^{-3}$	$W_{-2.5V}$ (μm)	$N_2(0.8\mu\text{m})$ $\times 10^{15} \text{cm}^{-3}$	W_0 (μm)	$N_1(W(0))$ $\times 10^{15} \text{cm}^{-3}$	$W_{-2.5V}$ (μm)	$N_2(0.8\mu\text{m})$ $\times 10^{15} \text{cm}^{-3}$
300	0.69	8.54	0.85	15.3	0.24	10.1	0.54	10.33
275	0.70	8.54	0.83	23.7	0.26	7.89	0.60	12.3
250	0.81	11.2	0.90	36.0	0.29	5.17	0.65	14.3
225	0.82	11.9	0.91	36.1	0.31	4.96	0.66	15.7
200	0.83	13.3	0.92	36.8	0.35	4.51	0.69	13.6
175	0.87	15.7	0.94	42.3	0.39	5.29	0.70	12.7

3.6 Current Transport Processes in Nanowire CdS/CdTe Solar Cells

To gain deeper insight into the nature of electron transport across the nanowire CdS-CdTe heterojunction, and to identify the processes which limit device performance in these solar cells, I-V characteristics of a typical nanowire device were measured at different temperatures in the 300 °K -175 °K range. Figure 6B shows variations with temperature in the values of diode ideality factor, A and α ($= q/AkT$). It is interesting to note that the value of A is greater than 2, and increases from 2.56 to 3.98 and from 4.5 to 7.4 in the dark and in light, respectively, as the device temperature is reduced from 300 °K to 175 °K . The slope α ($\alpha= q/AkT$) varies slightly with temperature, between 15.4 and 16.7 in the dark, and between 8.3 and 8.87 in the light. According to the theoretical models developed earlier[43],

it is the sequence of tunnelling current and the interface recombination current, which can lead to the α being independent of temperature and the diode ideality factor (A) being in excess of 2.

Figure 6D illustrates schematically the two electron transport processes at the nanowire CdS-CdTe heterojunction. These are, (i) tunnelling of electrons from n-CdS nanowires, across the narrow CdS depletion layer region to the interface states, followed by trickling down the interface states until they reach the top of the CdTe valance band and recombine with holes; and, (ii) tunnelling of electrons from n-CdS nanowires, across the narrow CdS depletion layer region to the mid-gap trap levels in CdTe, followed by recombination with holes in the valance band of CdTe [44]. For illustration, the other two less dominant processes involving the diffusion of electrons from CdS followed by recombination in CdTe are also shown in Figure 6D. The latter two are less dominant because they are associated with A being less than 2. Thus, it appears that the densities of interface states and traps enable the tunnelling-recombination processes over the electron transport processes of diffusion followed by bulk or space charge layer (SCL) recombination.

Table 2: J_0 and V_{oc} of a nanowire CdS/CdTe solar cell at various temperatures.

T(K)	J_0 (A/cm²)	V_{oc} (mV)
300	5.5×10^{-8}	770
275	3.8×10^{-8}	800
250	1.6×10^{-8}	840
225	3.3×10^{-9}	875
200	6.1×10^{-10}	910
175	1.3×10^{-10}	940

Temperature dependence of V_{oc} provides another valuable tool for determining the performance limit of solar cells, whereby the activation energy, E_a of the dominant recombination mechanism can

be extracted through the literature [45]. Figure 6C shows a plot of V_{oc} versus T , which, when extrapolated to $T=0$, yields a value of 1.19 eV for E_a . The fact that this number is smaller than 1.45 eV, the energy band gap of CdTe, is another indication that, because of the non-ideal electron transport processes such as tunnelling and interface recombination at the junction, the V_{oc} of nanowire CdS-CdTe solar cell remains smaller than what it can be.

Table 2 shows the variations in J_o and V_{oc} of the nanowire CdS/CdTe solar cell with decreasing temperature. When J_o decreases from $5.5 \times 10^{-8} \text{ A/cm}^2$ at 300 °K to $3.3 \times 10^{-9} \text{ A/cm}^2$ at 225 °K, the corresponding V_{oc} increases from 770 mV to 875 mV. This suggests a pathway to improve the V_{oc} in the future. Traps and interface state density needs to be reduced so that the value of J_o at room temperature can be brought down to 10^{-9} A/cm^2 , and the value of V_{oc} increased to 875 mV. This can be accomplished by optimization of CdS nanowire layer and the CdTe absorber layer (high vacuum of 0.02torr), avoidance of high resistivity buffer layer of intrinsic SnO_2 , and integration with the several conventional approaches, such as utilizing high conductivity and transparent substrates and applying low resistance back contacts.

4. Conclusions

Nanowire CdS-CdTe solar cell device structures were investigated for increasing the quantum efficiency and the power conversion efficiency of the CdS-CdTe solar cells. CdS nanowires embedded in AAO membranes with occupancy ratio of 32% were used to tailor optical properties and enable light transmission gain especially in the 300nm to 550nm wavelength range. Light spectrum directed into absorber layer was thus extended and light absorption loss at short wavelength improved. A nearly ideal spectral response of quantum efficiency from 300 nm to 860 nm, the bandgap edge of CdTe, provided evidence for improved light transmission through the window layer and enhanced carrier generation and collection in the CdTe absorber layer. A nanowire CdS/CdTe solar cell with Cu/graphite/Silver paste as back contact, on SnO_2 /ITO-soda lime glass substrates, with no additional

antireflection coating, yielded power conversion efficiency of 12% under 1sun illumination. In addition, with MoO_{3-x} /Au back contacts, the nanowire CdS-CdTe solar cells exhibited efficiency comparable to the efficiency of planar counterparts. The observed photocurrent value of 26 mA/cm^2 is substantially higher than that of core-shell nanopillar CdS-CdTe solar cells. V_{oc} of 770 mV value is significantly higher than V_{oc} (620mV) of core-shell nanopillar CdS-CdTe solar cells, and window layer band gap widening cells (670mV-710mV). Interface states, deep traps and current transport are identified for further improvement in V_{oc} and efficiency. This could be done with the optimization of CdS nanowires and CdTe characteristics and interface passivation and reducing series resistance at the back contacts. This nanowire window layer design offers an opportunity for other optoelectronic devices to enhance light transmission through nanostructures. Further, this nanowire device concept is applicable not only to the CdS-CdTe but also to other window-absorber type solar cells like CdS-CIGS and CdS-CZTSSe.

.....

AUTHOR INFORMATION

Corresponding Author

*E-mail: vsingh@uky.edu Tel: +1-859-979-1525

Author Contributions

H.D. designed and conducted the experiments, fabricated the nanowire solar cells, performed characterizations and simulations and analyzed data. V.S. originally conceived these nanowire solar cell device designs, planned the overall study and analyzed results of measurements. H.D. and V.S. wrote the manuscript. S.G. and J.H. contributed to the electro-optical characterizations.

Notes

The authors declare no competing financial interest.

Acknowledgments

This work was supported in part by grants from the National Science Foundation, (NSF-NIRT-ECS-0609064) and (NSF-EPCOR EPS-0447479), Department of Energy / Kentucky Renewable Energy Consortium (DE-FG36-05G085013/ULRF 05-1231G, (NSF-EPS-0447479) and by grants from the Kentucky Science and Engineering Foundation, (KSEF-148-502-02-27, KSEF- 148-502-03-68). The authors would like to thank PV measurements, Inc. for quantum efficiency measurement, and Dr. Suresh Rajaputra for SEM images.

References

- [1] W.U. Huynh, J.J. Dittmer, A.P. Alivisatos, Hybrid nanorod-polymer solar cells, *science*, 295 (2002) 2425-2427.
- [2] M.M. Lee, J. Teuscher, T. Miyasaka, T.N. Murakami, H.J. Snaith, Efficient hybrid solar cells based on meso-superstructured organometal halide perovskites, *Science*, 338 (2012) 643-647.
- [3] J. Oh, H.-C. Yuan, H.M. Branz, An 18.2%-efficient black-silicon solar cell achieved through control of carrier recombination in nanostructures, *Nature nanotechnology*, 7 (2012) 743-748.
- [4] H. Xin, O.G. Reid, G. Ren, F.S. Kim, D.S. Ginger, S.A. Jenekhe, Polymer nanowire/fullerene bulk heterojunction solar cells: how nanostructure determines photovoltaic properties, *Acs Nano*, 4 (2010) 1861-1872.
- [5] G. Ren, P.-T. Wu, S.A. Jenekhe, Solar cells based on block copolymer semiconductor nanowires: effects of nanowire aspect ratio, *ACS nano*, 5 (2010) 376-384.
- [6] J.H. Heo, S.H. Im, J.H. Noh, T.N. Mandal, C.-S. Lim, J.A. Chang, Y.H. Lee, H.-j. Kim, A. Sarkar, M.K. Nazeeruddin, Efficient inorganic-organic hybrid heterojunction solar cells containing perovskite compound and polymeric hole conductors, *Nature photonics*, 7 (2013) 486-491.
- [7] M. Law, L.E. Greene, J.C. Johnson, R. Saykally, P. Yang, Nanowire dye-sensitized solar cells, *Nature materials*, 4 (2005) 455-459.
- [8] J.B. Baxter, E.S. Aydil, Nanowire-based dye-sensitized solar cells, *Applied Physics Letters*, 86 (2005) 053114.
- [9] B. O'regan, M. Grätzel, A low-cost, high-efficiency solar cell based on dye-sensitized, *nature*, 353 (1991) 737-740.
- [10] J. Qi, X. Dang, P.T. Hammond, A.M. Belcher, Highly efficient plasmon-enhanced dye-sensitized solar cells through metal@ oxide core-shell nanostructure, *ACS nano*, 5 (2011) 7108-7116.
- [11] B. Tian, X. Zheng, T.J. Kempa, Y. Fang, N. Yu, G. Yu, J. Huang, C.M. Lieber, Coaxial silicon nanowires as solar cells and nanoelectronic power sources, *Nature*, 449 (2007) 885-889.
- [12] M.D. Kelzenberg, S.W. Boettcher, J.A. Petykiewicz, D.B. Turner-Evans, M.C. Putnam, E.L. Warren, J.M. Spurgeon, R.M. Briggs, N.S. Lewis, H.A. Atwater, Enhanced absorption and carrier collection in Si wire arrays for photovoltaic applications, *Nature materials*, 9 (2010) 239-244.
- [13] L. Kranz, C. Gretener, J. Perrenoud, R. Schmitt, F. Pianezzi, F. La Mattina, P. Blösch, E. Cheah, A. Chirilă, C.M. Fella, Doping of polycrystalline CdTe for high-efficiency solar cells on flexible metal foil, *Nature communications*, 4 (2013) 1-7.
- [14] X. Wu, High-efficiency polycrystalline CdTe thin-film solar cells, *Solar energy*, 77 (2004) 803-814.
- [15] P. Jackson, D. Hariskos, E. Lotter, S. Paetel, R. Wuerz, R. Menner, W. Wischmann, M. Powalla, New world record efficiency for Cu (In, Ga) Se₂ thin-film solar cells beyond 20%, *Progress in Photovoltaics: Research and Applications*, 19 (2011) 894-897.
- [16] T.K. Todorov, J. Tang, S. Bag, O. Gunawan, T. Gokmen, Y. Zhu, D.B. Mitzi, Beyond 11% Efficiency: Characteristics of State-of-the-Art Cu₂ZnSn (S, Se) 4 Solar Cells, *Advanced Energy Materials*, 3 (2013) 34-38.
- [17] L. Kosyachenko, E. Grushko, X. Mathew, Quantitative assessment of optical losses in thin-film CdS/CdTe solar cells, *Solar Energy Materials and Solar Cells*, 96 (2012) 231-237.
- [18] C. Ferekides, U. Balasubramanian, R. Mamazza, V. Viswanathan, H. Zhao, D. Morel, CdTe thin film solar cells: device and technology issues, *Solar Energy*, 77 (2004) 823-830.
- [19] G. Kartopu, A.J. Clayton, W.S. Brooks, S.D. Hodgson, V. Barrioz, A. Maertens, D.A. Lamb, S.J. Irvine, Effect of window layer composition in Cd_{1-x}Zn_xS/CdTe solar cells, *Progress in Photovoltaics: Research and Applications*, 22 (2014) 18-23.
- [20] K.D. Dobson, I. Visoly-Fisher, G. Hodes, D. Cahen, Stabilizing CdTe/CdS Solar Cells with Cu-Containing Contacts to p-CdTe, *Advanced Materials*, 13 (2001) 1495-1499.

- [21] Z. Fan, H. Razavi, J.-w. Do, A. Moriwaki, O. Ergen, Y.-L. Chueh, P.W. Leu, J.C. Ho, T. Takahashi, L.A. Reichertz, Three-dimensional nanopillar-array photovoltaics on low-cost and flexible substrates, *Nature materials*, 8 (2009) 648-653.
- [22] P. Liu, V.P. Singh, C.A. Jarro, S. Rajaputra, Cadmium sulfide nanowires for the window semiconductor layer in thin film CdS–CdTe solar cells, *Nanotechnology*, 22 (2011) 145304.
- [23] J.S. Suh, J.S. Lee, Surface enhanced Raman scattering for CdS nanowires deposited in anodic aluminum oxide nanotemplate, *Chemical Physics Letters*, 281 (1997) 384-388.
- [24] H. Dang, S. Rajaputra, J. Chen, S. Guduru, N. Reddy, E. Krause, J. Church, V. Singh, CdS nanowire layers of enhanced transmittance for window layer applications in thin film solar cells, *Photovoltaic Specialists Conference (PVSC)*, 38th IEEE, (2012) 002697-002701.
- [25] Y.-J. Lee, D.S. Ruby, D.W. Peters, B.B. McKenzie, J.W. Hsu, ZnO nanostructures as efficient antireflection layers in solar cells, *Nano letters*, 8 (2008) 1501-1505.
- [26] M.-J. Huang, C.-R. Yang, Y.-C. Chiou, R.-T. Lee, Fabrication of nanoporous antireflection surfaces on silicon, *Solar Energy Materials and Solar Cells*, 92 (2008) 1352-1357.
- [27] T. Nakada, M. Mizutani, 18% efficiency Cd-free Cu (In, Ga) Se₂ thin-film solar cells fabricated using chemical bath deposition (CBD)-ZnS buffer layers, *Japanese Journal of Applied Physics*, 41 (2002) L165.
- [28] K. Ramanathan, M.A. Contreras, C.L. Perkins, S. Asher, F.S. Hasoon, J. Keane, D. Young, M. Romero, W. Metzger, R. Noufi, Properties of 19.2% efficiency ZnO/CdS/CuInGaSe₂ thin-film solar cells, *Progress in Photovoltaics: Research and Applications*, 11 (2003) 225-230.
- [29] I. Repins, M.A. Contreras, B. Egaas, C. DeHart, J. Scharf, C.L. Perkins, B. To, R. Noufi, 19.9%-efficient ZnO/CdS/CuInGaSe₂ solar cell with 81.2% fill factor, *Progress in Photovoltaics: Research and applications*, 16 (2008) 235-239.
- [30] D.A.R. Barkhouse, O. Gunawan, T. Gokmen, T.K. Todorov, D.B. Mitzi, Device characteristics of a 10.1% hydrazine-processed Cu₂ZnSn (Se, S) 4 solar cell, *Progress in Photovoltaics: Research and Applications*, 20 (2012) 6-11.
- [31] S. Ahmed, K.B. Reuter, O. Gunawan, L. Guo, L.T. Romankiw, H. Deligianni, A high efficiency electrodeposited Cu₂ZnSnS₄ solar cell, *Advanced Energy Materials*, 2 (2012) 253-259.
- [32] T.K. Todorov, K.B. Reuter, D.B. Mitzi, High-Efficiency Solar Cell with Earth-Abundant Liquid-Processed Absorber, *Advanced materials*, 22 (2010) E156-E159.
- [33] A. Chirilă, S. Buecheler, F. Pianezzi, P. Bloesch, C. Gretener, A.R. Uhl, C. Fella, L. Kranz, J. Perrenoud, S. Seyrling, Highly efficient Cu (In, Ga) Se₂ solar cells grown on flexible polymer films, *Nature materials*, 10 (2011) 857-861.
- [34] B.M. Başol, B. McCandless, Brief review of cadmium telluride-based photovoltaic technologies, *Journal of Photonics for Energy*, 4 (2014) 040996-040996.
- [35] M.A. Green, K. Emery, Y. Hishikawa, W. Warta, E.D. Dunlop, Solar cell efficiency tables (Version 45), *Progress in photovoltaics: research and applications*, 23 (2015) 1-9.
- [36] W. Yang, H.S. Duan, B. Bob, H. Zhou, B. Lei, C.H. Chung, S.H. Li, W.W. Hou, Y. Yang, Novel Solution Processing of High-Efficiency Earth-Abundant Cu₂ZnSn (S, Se) 4 Solar Cells, *Advanced Materials*, 24 (2012) 6323-6329.
- [37] D.H. Rose, F.S. Hasoon, R.G. Dhere, D.S. Albin, R.M. Ribelin, X.S. Li, Y. Mahathongdy, T.A. Gessert, P. Sheldon, Fabrication procedures and process sensitivities for CdS/CdTe solar cells, *Progress in Photovoltaics Research and Applications*, 7 (1999) 331-340.
- [38] N.R. Paudel, A.D. Compaan, Y. Yan, Ultrathin CdTe Solar Cells with MoO₃-x/Au Back Contacts, *Journal of Electronic Materials*, (2014) 1-5.
- [39] N. Paudel, A. Compaan, Y. Yan, Sputtered CdS/CdTe solar cells with MoO_{3-x}/Au back contacts, *Solar Energy Materials and Solar Cells*, 113 (2013) 26-30.
- [40] H. Lin, W. Xia, H.N. Wu, C. Tang, CdS/CdTe solar cells with MoO_x as back contact buffers, *Applied Physics Letters*, 97 (2010) 123504-123503.
- [41] A. Balcioglu, R. Ahrenkiel, F. Hasoon, Deep-level impurities in CdTe/CdS thin-film solar cells, *Journal of Applied Physics*, 88 (2000) 7175-7178.
- [42] F.H. Seymour, V. Kaydanov, T.R. Ohno, D. Albin, Cu and CdCl₂ influence on defects detected in CdTe solar cells with admittance spectroscopy, *Applied Physics Letters*, 87 (2005) 153507.

- [43] V.P. Singh, D.L. Linam, D. Dils, J.C. McClure, G. Lush, Electro-optical characterization and modeling of thin film CdS–CdTe heterojunction solar cells, *Solar energy materials and solar cells*, 63 (2000) 445-466.
- [44] H. Dang, V. Singh, S. Rajaputra, S. Guduru, J. Chen, B. Nadimpally, Cadmium sulfide nanowire arrays for window layer applications in solar cells, *Solar Energy Materials and Solar Cells*, 126 (2014) 184-191.
- [45] S.S. Hegedus, W.N. Shafarman, Thin-film solar cells: device measurements and analysis, *Progress in Photovoltaics: Research and Applications*, 12 (2004) 155-176.

GRAPHICAL ABSTRACT

Embedded CdS nanowires are used for improving spectral transmission and increasing the mechanical and electrical robustness of CdS window layer, thus enhancing the quantum efficiency and the reliability of CdS-CdTe solar cells. Nanowire CdS/CdTe solar cells with Cu/graphite/silver paste as back contacts, on SnO_2 /ITO-soda lime glass substrates, yield the highest efficiency of 12% in nanostructured CdS-CdTe solar cells.