Influence of oxidation temperature on the interfacial properties of n-type 4H-SiC MOS capacitors

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The effect of oxidation temperature on interfacial properties of n-type 4H-SiC metal-oxide-semiconductor capacitors has been systematically investigated. Thermal dry oxidation process with three different oxidation temperatures 1200 °C, 1300 °C and 1350 °C were employed to grow SiO₂ dielectric, following by the standard post-oxidation annealing (POA) in NO ambience at 1175 °C for 2 hrs. The root mean square (RMS) roughness measured by Atomic Force Microscopy for the thermally grown SiO₂ before POA process is reduced with increasing the oxidation temperature, obtaining an atomically flat surface with a RMS of 0.157 nm from the sample oxidized at 1350 °C. Several kinds of electrical measurements were used to evaluate the densities of near interface traps and effective fixed dielectric charge for the samples, exhibiting a trend reduced with increasing the oxidation temperature. The interface state density of $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.2eV from the conduction band edge was achieved from conductance method measurement for the sample oxidized at 1350 °C. The results from Secondary Ion Mass Spectroscopy and X-ray Photoelectron Spectroscopy demonstrate that high oxidation temperature can reduce the width of transition layer, the excess Si and silicon suboxide compositions near the

interface, leading to effective improvement of the interfacial properties.

Keywords: 4H-SiC MOS capacitors, thermal oxidation temperature, interfacial properties, effective fixed dielectric charge, near interface traps, interface states

1. Introduction

Silicon carbide (SiC) metal-oxide-semiconductor field-effect transistors (MOSFETs) are expected to replace Si-based MOSFETs for high-temperature and high-power applications, owing to its superior material properties such as high critical breakdown electric field strength, high electron saturation velocity and high thermal conductivity. Besides its excellent properties, only stable silicon dioxide (SiO₂) insulator on SiC can be grown by conventional thermal oxidation process, which makes fabricate SiC metal-oxide-semiconductor (MOS) devices far more easily compared with the other wide band gap semiconductors.

Although the 4H-SiC MOSFETs are already commercial available for a few years, the SiO₂/SiC interface quality and oxide reliability are still the key issues limiting the development of the high performance 4H-SiC MOSFETs [1-4]. Such high density of charge traps near the interface seriously degrade the channel mobility of the SiC MOSFET, resulting in a higher on-resistance and the threshold-voltage instability and restricting the wide band gap advantage of 4H-SiC [1,2]. The previous researches mainly focused on the effect of the different POA processes on improvements of SiO₂/SiC interface system, such as POA in nitrogen or phosphorus containing ambience, and showed that the nitrogen and phosphorus based annealing can effectively improve the interface quality [5-8]. However, in addition to the POA treatment process, the impact of the oxidation temperature on the SiO₂/SiC interface quality is also required to further research. The previous thermal oxidation processes for 4H-SiC were typically performed at the maximum operating temperature of 1200 °C in the common quartz furnace, so the oxidation at higher than 1200 °C becomes attractive. Recent reports on the high-temperature oxidations (> 1200 °C) of 4H-SiC have shown that the density of interface states (D_{it}) can be decreased [9-14].

The influence of the thermal oxidation temperature on D_{it} was reported in 2006 by Kurimoto et al [9]. The work reported by Kikuchi et al showed a very low D_{it} in a 14 nm oxide thickness sample by thermal oxidation at 1300 °C with O₂ annealing, in which the temperature window for the ideal reaction of SiC thermal oxidation in O₂ ambience with a standard atmospheric pressure was approximately estimated to be 1100~1400 °C [10,11]. Recently, higher oxidation temperature up to 1400 °C was also used to form the SiO₂ reported by Naik et al [12], however the results processed in 1400 °C were not as good as the expectation of better mobility at such higher oxidation temperature, and a channel mobility of corresponding MOSFETs was only 2 cm²/Vs. In this case, Ref. [15] reported that the oxidation process with higher than 1400 °C enhances interstitial C injecting into SiC, resulting in large amounts of scattering centers as well as traps in the SiC inversion channel. Although great effort has been made on SiC high temperature oxidation and a number of studies on the effect of the oxidation temperature on the density of interface states has been reported, there is not enough information about the influence of the high oxidation temperature on near interface traps (NITs) and effective fixed dielectric charge (N_{eff}). Recent works have shown the existence of a kind of NITs in the SiC MOS devices, which can exchange charge with the semiconductor easily and could significantly affect the channel mobility [16,17]. However, the relationship of NITs with the oxidation temperature in the 4H-SiC MOS devices is still not very clear. Therefore, the further investigation is required for the mechanism of oxidation temperature influence on the NITs and N_{eff} of 4H-SiC MOS devices.

In this paper, three different high oxidation temperatures 1200 °C, 1300 °C and 1350 °C were employed to grow SiO₂ dielectric on n-type 4H-SiC to figure out the effects of high oxidation temperature on the SiO₂/SiC interface characteristics and quality of SiO₂ film, and the improvement mechanism of interfacial characteristics is further investigated by Atomic Force Microscopy (AFM), capacitance-voltage (C-V), conductance-frequency (G-f), current-voltage (I-V), Secondary Ion Mass Spectroscopy (SIMS) and X-ray Photoelectron Spectroscopy (XPS) measurements.

2. Experimental methods

4H-SiC wafer with an epitaxial layer thickness of 13 μm and nitrogen-doped concentration of $7.8 \times 10^{15} \text{ cm}^{-3}$, grown on silicon faced 4° off-axis n-type substrate purchased from EpiWorld International Co., Ltd., was used in this experiment. Following the RCA cleaning, a HF dip and water rinsing, thermal oxidation was carried out in dry O_2 environment at temperatures of 1200 $^\circ\text{C}$ (180 min), 1300 $^\circ\text{C}$ (30 min) and 1350 $^\circ\text{C}$ (15 min), respectively. The surface morphological properties of thermally grown SiO_2 were assessed by Keysight 5500 Atomic Force Microscopy after the high-temperature oxidation processes. Besides, the C-V characteristics before POA were measured by Hg probe test platform in clean room using the duplicate samples, which were cut from the same wafer and oxidized in the same furnace. Afterwards, all of the samples without Hg probe test were annealed using the conventional NO annealing process (1175 $^\circ\text{C}$ for 2 hours). The thermal processing steps are summarized for all samples in Table. 1. The oxide thicknesses (d_{ox}) measured by J.A.Woollam M2000D spectroscopy ellipsometry (SE) were 49 nm, 51 nm and 57 nm for the samples oxidized at 1200 $^\circ\text{C}$, 1300 $^\circ\text{C}$ and 1350 $^\circ\text{C}$, respectively. Finally, MOS capacitor structure was fabricated, Ni was evaporated for the backside ohmic contact and Al was sputtered on the oxide surface to form the gate electrode.

Table.1. Thermal processing steps used for each of the samples.

Samples	Thermal oxidation	NO annealing
1200 $^\circ\text{C}$	@1200 $^\circ\text{C}$ (180 min)	@1175 $^\circ\text{C}$ (120 min)
1300 $^\circ\text{C}$	@1300 $^\circ\text{C}$ (30 min)	@1175 $^\circ\text{C}$ (120 min)
1350 $^\circ\text{C}$	@1350 $^\circ\text{C}$ (15 min)	@1175 $^\circ\text{C}$ (120 min)

Electrical characteristics of the samples in this study were measured on a CASCADE probe station, using a Keysight B1505A Semiconductor Parameter Analyzer. The SiO_2/SiC interface characteristics were evaluated by high frequency bidirectional capacitance-voltage and accumulation conductance–frequency measurements. The densities of near interface traps were extracted from the hysteresis

of the bidirectional C-V curves and the densities of interface states were determined by the conductance method. Gate oxide integrity (GOI) was evaluated by I-V measurements, and the forward I-V measurements were performed at room temperature by sweeping the leakage current up to 100 nA. The density of incorporated nitrogen and the relative contents of Si, O and C in the samples were determined by SIMS measurements in Evans Analytical Group (EAG) laboratories, and the width of the transition layer was extracted from the SIMS profile. The chemical bonding states at the interface were examined via Thermo Scientific X-ray Photoelectron Spectroscopy, in which a monochromatic Al K α X-ray excitation ($h\nu=1486.68$ eV) was used at a takeoff angle of 90° on the different samples. Argon ion sputtering was carried out in the same ultrahigh-vacuum chamber to remove the SiO₂ layer gradually.

3. Results and discussion

3.1. Surface morphology

Fig. 1. Typical surface morphology measured by AFM on the 4H-SiC epitaxial layer (a) before oxidation and the SiO₂ films oxidized at (b) 1200 °C, (c) 1300 °C and (d) 1350 °C before POA process

Firstly, the surface morphology of the 4H-SiC epitaxial layer before oxidation process and the SiO₂ prepared with different oxidation temperatures were examined by AFM with testing area of $5 \times 5 \mu\text{m}^2$ and $10 \times 10 \mu\text{m}^2$. It is found that the statistical value of RMS and the maximum roughness for a given sample with different scan area are similar, so for the testing with better resolution, the typical results from testing area of $5 \times 5 \mu\text{m}^2$ are shown in Fig. 1. A smooth morphology (RMS=0.139 nm) was observed on the SiC epitaxial surface before oxidation process (Fig. 1(a)), in which the maximum roughness is below 1.3 nm. Comparing with the 4H-SiC epitaxial layer, the values of surface RMS for the three grown SiO₂ samples become larger. Besides, it is found that there are some protuberances with the peak height about 3.7 nm on the surface of the three oxidized samples. Moreover, the numbers of the protuberances are gradually reduced with increasing oxidation temperature. The surface morphological images exhibit that the value of RMS is related with the protuberances. Under 1200 °C oxidation condition (Fig. 1(b)), the RMS roughness is 0.379 nm and large numbers of the protuberances are observed. The sample oxidized at 1300 °C (Fig. 1(c)) shows a RMS roughness of 0.231 nm with several isolated surface protuberances. In the case oxidized at 1350 °C, as shown in Fig. 1(d), there is only one obvious protuberance observed at the edge of the $5 \times 5 \mu\text{m}^2$ testing area. Thus, it is found that an atomically flat surface with a RMS roughness of only 0.157 nm is achieved and protuberances are

almost successfully eliminated by high temperature oxidation process at 1350 °C. It is inferred that the surface protuberances may be related to the lattice mismatch of some incompletely reacted atoms and the higher oxidation temperature may help to restrain the formation of this kind of protuberances. In addition, it is worth noting that the peak heights of the protuberances for all of the samples are reduced into less than 2 nm after POA in NO ambience (not shown here). It is suggested that the NO POA induces a slow re-oxidation process and high-temperature condition may help the surface atoms to be redistributed, thus improving the surface morphology compared with the original thermal oxidation.

3.2. *Effective fixed dielectric charge*

Fig. 2(a) shows the normalized capacitance-voltage characteristics of the three samples, in which C-V data were measured from the fabricated MOS capacitors at the frequency of 10 kHz at room temperature (300K). For comparisons, the ideal C-V curve (dashed line) calculated by solving Poisson's equation is also inserted in Fig. 2(a), indicating that the different temperature oxidation processes make the different flat-band voltage positive shifts. The flat-band voltage shift (ΔV_{FB}) from the ideal value can be used to obtain the density of effective fixed dielectric charge [18], and the extracted N_{eff} before and after the post-oxidation annealing process are shown in Fig. 2(b). It is obvious that the density of N_{eff} is decreased with the increase of the oxidation temperature and the NO POA process can effectively reduce the negative fix charge for all the three samples. Some reports have pointed out that the negative fixed charges are corresponding to the existence of carbon-related residua in the generated SiO₂ insulator [18,19]. Thus, it is considered that the reduction of N_{eff} with increasing the oxidation temperature is due to the reduction of residual carbon-related byproduct in the dielectric films in the higher temperature oxidation process. Besides, it is thought that the NO annealing induces a slow re-oxidation process to consume the carbon-related residua in the SiO₂ insulator and lead to the reduction of the density of N_{eff} .

Fig. 2. (a) Normalized C-V characteristics for the samples oxidized at different temperatures with NO POA. (b) The extracted negative N_{eff} before and after NO POA.

3.3. Near interface traps

Fig. 3(a) shows the normalized bidirectional capacitance-voltage characteristics of the three samples. In the measurements, the gate voltage was swept from depletion to accumulation, and then swept back to depletion at the frequency of 10 kHz at room temperature (300K).

Fig. 3. (a) Bidirectional C-V, (b) transient current and (c) accumulation

conductance-frequency characteristics of the three samples with different oxidation temperatures.

Table.2. Extracted electrical parameters of SiO₂/SiC MOS structures fabricated with different oxidation temperatures.

Oxidation Temperature (°C)	ΔV (V)	Areal density of NITs extracted from C-V hysteresis (cm ⁻²)	Volume density of NITs extracted from transient current (cm ⁻³)
1200	0.21	8.74×10^{10}	3.17×10^{19}
1300	0.14	5.16×10^{10}	1.41×10^{19}
1350	0.11	3.63×10^{10}	8.26×10^{18}

From Fig. 3(a), it can be observed that the hysteresis voltages (ΔV) all appear in the bidirectional C-V curves of the three samples, which is related to the charge traps near the interface of SiO₂/SiC. It is considered that electrons, majority carriers of n-type SiC substrate, are injected into the NITs during the forward C-V measurement (from depletion to accumulation). The areal density of NITs that are switching charge state to create the hysteresis observed can be calculated by $(C_{ox}/qS) \cdot \Delta V$ (shown in Table.2) [4]. Moghadam et al. proposed that the active NITs with energy levels aligned to the conduction band can be quantified by the transient current method [17]. Based on C-V results, the gate voltage was held at 5 V for 30 s. then, the gate voltage was stepped to 20 V and the transient current was measured. The resulted transient current, shown in Fig. 3(b), can be attributed to direct tunneling of electrons to the active NITs and the volume density of NITs can be estimated from the measured current (shown in Table.2) [17,20]. It is clearly shown that all the extracted density of NITs is decreased with increasing the oxidation temperature, which may be correlated with the reduction of silicon enrichment or oxygen deficiency near the interface. Besides, Haasmann et al. demonstrated that the accumulation conductance characteristics over a range of frequency can provide detailed information on both the density and distribution of the NITs in SiO₂/SiC MOS structures [16,21]. Therefore, the accumulation conductance-frequency characteristics of the samples were measured from 1 kHz to 100 kHz at a moderate oxide electric field of 1.5 MV/cm, as shown in Fig. 3(c). It can

be seen that all the accumulation conductance plots exhibit strong frequency dependence. The tendency of the accumulation conductance increases at higher frequencies, indicating that the density of NITs closer to the SiO₂/SiC interface is increased. Moreover, the SiO₂ sample grown with higher temperature oxidation process shows a prominent reduction of NITs throughout the measurement frequency range, which is consistent with the results deduced from the hysteresis of bidirectional C-V curves and transient current (in the Table.2).

3.4. Density of interface states

Conductance measurements were performed at frequencies from 1 kHz to 2 MHz at room temperature with a small signal voltage of 30 mV. Fig. 4(a) shows the normalized parallel conductance (G_p/ω) data for the sample oxidized at 1300 °C. Series resistance was extracted by measuring the impedance under accumulation bias and then subtracted from the measured data [22]. Energy level with reference to the conduction band edge of 4H-SiC was calculated using surface potential based on depletion capacitance [23]. Since the Gaussian distribution of G_p/ω , which are dependent on the frequency range from 1 kHz to 2 MHz in our experiment, are directly related to the capacitance of interface traps. D_{it} are approximately calculated from the maximum value of G_p/ω [10], as shown in Fig. 4(b).

Fig. 4. (a) The normalized parallel conductance as a function of angular frequency and energy level with reference to the conduction band edge of SiC for the sample oxidized at 1300 °C. (b) Energy distribution of interface state density for N-type 4H-SiC MOS capacitors of the samples oxidized at different temperatures.

Fig. 4(b) shows that the densities of interface states are decreased with the oxidation temperature from 1200 °C to 1350 °C. The lowest D_{it} , $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.2 eV from the conduction band edge is achieved for the sample oxidized at 1350 °C followed by NO POA at 1175 °C. These results indicate that the density of interface states can be decreased by elevating the oxidation temperature and holding the same annealing condition. The effects of thermal oxidation temperature on the electrical performance of the interface states are similar to the previously reported results [11,12,14]. It is considered that the higher oxidation temperature can effectively reduce the accumulation of residual byproduct at the SiO_2/SiC interface.

3.5. Gate oxide integrity

Fig. 5. Typical current versus electric field (I-E) of fabricated N-type 4H-SiC MOS structure samples.

To evaluate the GOI, the forward I-V characteristics were measured at room temperature by sweeping the leakage current up to the compliance current of 100nA. Fig. 5 shows the forward current-electric versus field (I-E), which is transformed from the measured I-V characteristics. It is apparent that the I-E curves of the three samples exhibit similar behavior, typically complying with Fowler-Nordheim (F-N) rule. When the field strength is higher than 6 MV/cm, the electrons pass through the barrier between SiO_2 and substrate are controlled by F-N tunneling current, and the current increases exponentially with the applied electric field. Besides, the breakdown field

strength of the SiO_2 dielectric film must be higher than 8.7MV/cm for all the three samples at room temperature. Thus, it is importantly observed that the higher temperature oxidation process with a faster oxidation rate does not make the GOI degraded. On the contrary, the tunneling current shows a little dependence on the oxidation temperature, as shown in the inset of Fig. 5.

3.6. Secondary Ion Mass Spectroscopy measurements

In order to investigate the mechanism of oxidation temperature influence on SiO_2/SiC interfacial properties, SIMS was performed to examine the components of the different samples, as shown in Fig. 6.

Fig. 6. (a) SIMS profiles for the NO annealed MOS capacitor with the oxidation temperature of 1300 °C. Transition layer width extracted from O/Si and C/Si composition ratio curves and the excess Si relative content vs. depth for the samples oxidized at (b) 1200 °C, (c) 1300 °C and (d) 1350 °C.

It is worth noting that Si is accumulated near the interface and a small accumulation peak is formed for all the three different samples, as shown in Fig. 6(a)

(red arrow). The silicon relative content in the accumulation peak is even more than that in the SiC epi-layer. Thus, the relative content of excess Si is obtained by the content of silicon minus the content of carbon and half of oxygen. In Figs. 6(b)~(d), the transition layer width extracted from the SIMS profile are about 7.58 nm, 6.65 nm and 6.4 nm for the samples oxidized at 1200 °C, 1300 °C and 1350 °C, respectively, which defining the region between the pure SiO₂ and SiC. Besides, two Gaussian-like accumulation regions within the transition layer are caused by the excess Si and nitrogen, as shown in the NO annealed samples. The existence of excess silicon atoms in the transition layer provides the relevant evidence to verify the speculations in the previous reports that the near interface defects may be related to Si interstitials, strained Si–Si bonds and silicon suboxide [24-26]. Evidently, the Gaussian-like accumulation of N and excess Si atoms are aligned in the transition layer. It is suggested that some of the excess Si incorporate nitrogen to form strong Si≡N bonds in the transition layer during the NO annealing process, allowing better relaxation of the interface strain, leading to the observed NITs effective reduction by nitrogen passivation which conforms to Refs. [8,21,27]. Besides, the researches on different NO annealing time reported by Rozen et al. demonstrated that the interface characteristics were improved with the increase of annealing time and there was still room for further improvement, even with the annealing time up to 4 hours [28,29]. Thus, for the three samples oxidized at different temperatures with the unified NO POA process, the observed NITs are still originated from the excess silicon atoms, which have not been passivated completely by the 2 hours NO annealing process. Based on the SIMS data, Fig. 7 illustrates the silicon atoms content near the interface for the samples oxidized at different temperatures. It is clear that both the relative Si and excess Si content show the trend of decrease near the interface with increasing the oxidation temperature.

Fig. 7. (a) Relative Si and (b) excess Si content for the samples oxidized at different temperatures. Note: in order to make clear comparison, it is required to draw the results on the same plot, and their respective signal is dealt with aligned so that the peak values can be used to study the status at and near the SiO₂/SiC interfaces.

3.7. X-ray Photoelectron Spectroscopy measurements

Deconvolution of the Si 2p and N 1s core level XPS spectra has been performed to analyze the chemical bonding states at the interface for the different samples, as shown in Fig. 8(a) and (b). Before the curve fitting, Shirley background subtraction was performed and all spectra were charge compensated relative to the binding energy of the C-C bond (284.6 eV). Then, XPS spectra were resolved as sums of several components assuming that each peak has a Gaussian line shape. In Fig. 8(a) four main components are observed in the Si 2p spectra, that are Si-C, Si≡N, Si-O_x and Si-O₂ located at 100.4, 102.0, 102.7 and 103.8 eV binding energies [30,31], respectively. The Si-C near 100.4 eV and Si-O₂ near 100.8 eV are in good agreement with the values for pure stoichiometric phases of SiC and SiO₂ [32]. The peak near 102.7 eV corresponds to the intermediate oxidation state of Si-O_x, which is indicative of the unstable silicon suboxide near the SiO₂/SiC interface. Fig. 8(b) shows the corresponding N 1s core level spectra of the three samples. One main contribution can be identified due to N≡Si near 398.2 eV, indicating that the strong Si≡N bonds do exist near the interface [21,33], which is consistent with the results deduced from the SIMS profiles. Fig. 8(c) reveals the relative content of intermediate oxidation state (Si-O_x) in the Si 2p core level spectra for the samples oxidized at different temperatures, which is obtained by XPS analysis software (Thermo Advantage). It is shown that the contents of the silicon

suboxide are decreased with increasing the oxidation temperature, and the tendency is accorded with the change of excess Si content in SIMS results.

Fig. 8. Si 2p (a) and N 1s (b) core level XPS spectra for the SiO₂/SiC interface of the samples oxidized at different temperatures. (c) The relative contents of silicon suboxide in the Si 2p core level spectra for the different samples.

Up to now, it is clear that the width of transition layer, the excess Si and silicon suboxide compositions all show the decreased trend near the interface with increasing the oxidation temperature. Thus, based on the modified Deal-Grove thermal oxidation kinetics of SiC [34], it is suggested that high oxidation temperature can improve the transport rate in the grown SiO₂ film, not only enhancing the diffusion of molecular oxygen gas to the reaction surface but also removing the related byproducts away from the surface during the oxidation process, so this process increases oxidation rate, also makes the oxidation reaction more completely and reduces the transition layer width

and residual byproducts accumulation at and near the SiO₂/SiC interface.

4. Conclusions

The interfacial characteristics of thermally grown SiO₂/4H-SiC at temperatures of 1200 °C, 1300 °C and 1350 °C with POA in NO ambience have been systematically investigated. The AFM results before POA show that the RMS roughness is reduced when the oxidation temperature is increased, and an atomically flat surface with a RMS of 0.157 nm is obtained for the sample oxidized at 1350 °C. The results obtained from several kinds of electrical measurements indicate that the density of near interface traps and effective fixed dielectric charge can be effectively decreased by elevating the oxidation temperature, and the lowest density of D_{it} for the sample oxidation at 1350 °C is about $3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.2 eV from the conduction band edge. Besides, the I-V characteristics show that the GOI of thermally grown SiO₂ film is not degraded after the higher temperature oxidation process. The results from SIMS and XPS have revealed that the improvement of the interfacial characteristics at high oxidation temperature results from the reduction of the transition layer width, the excess silicon and silicon suboxide accumulation at and near the SiO₂/SiC interface, leading to effectively reducing the density of interface states and near interface traps and improving the interface quality.

Acknowledgements

The authors would like to appreciate the Zhuzhou CRRC Times Electric Co., Ltd. for using their high temperature oxidation facilities. This work was supported in part by National Key Basic Research Program of China (Grant No. 2015CB759600), National Science Foundation of China (Grant Nos. 61404098 and 61274079), Key Specific Projects of the Ministry of Education of China (Grant No. 625010101), and Doctoral Fund of the Ministry of Education of China (Grant No. 20130203120017).

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