Effective surface passivation of p-type crystalline silicon with silicon oxides formed by light-induced anodisation

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Abstract

Electronic surface passivation of p-type crystalline silicon by anodic silicon dioxide (SiO₂) was investigated. The anodic SiO₂ was grown by light-induced anodisation (LIA) in diluted sulphuric acid at room temperature, a process that is significantly less-expensive than thermal oxidation which is widely-used in silicon solar cell fabrication. After annealing in oxygen and then forming gas at 400 °C for 30 min, the effective minority carrier lifetime of 3-5 Ω cm, boron-doped Czochralski silicon wafers with a phosphorus-doped 80 Ω/□ emitter and a LIA anodic SiO₂ formed on the p-type surface was increased by two orders of magnitude to 150 μs. Capacitance-voltage measurements demonstrated a very low positive charge density of $3.4 \times 10^{11} \text{ cm}^{-2}$ and a moderate density of interface states of $6 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. This corresponded to a silicon surface recombination velocity of 62 cm s⁻¹, which is comparable with values reported for other anodic SiO₂ films, which required higher temperatures and longer growth times, and significantly lower than oxides grown by chemical vapour deposition techniques. Additionally, a very low leakage current density of 3.5×10^{-10} and $1.6 \times 10^{-9} \text{ A cm}^{-2}$ at 1 and -1 V, respectively, was measured for LIA SiO₂ suggesting its potential application as insulation layer in IBC solar cells and a barrier for potential induced degradation.

Keywords:

Anodisation, low-temperature processing, silicon dioxide, surface passivation

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Abbreviations:

CV: Capacitance-voltage

CVD: Chemical vapour deposition

Cz: Czochralski

ETP: Expanding thermal plasma

LIA: Light-induced anodisation

MOS: Metal-oxide-semiconductor

PID: Potential induced degradation

QSS-PL: Quasi steady state photoluminance

SRV: Surface recombination velocity

1. Introduction

Thermally-grown silicon dioxide (SiO_2) has been widely used to electronically passivate surfaces of silicon solar cells over the past few decades. The resulting high quality silicon- SiO_2 interface enables surface recombination velocity's (SRV) less than 30 cm s^{-1} [1] to be achieved. This has resulted in these films being used extensively in high efficiency silicon solar cell fabrication [2-4]. Thermal SiO_2 has also found application as a barrier layer under silicon nitride (SiN_x) antireflection coatings of silicon solar cells, which effectively avoids over-plating of metal through pinholes in the SiN_x [5]; a contact passivation layer [6-9] and can mitigate potential induced degradation (PID), where minimising leakage current through the antireflection coating is paramount [10]. However, the growth of thermal oxides requires long oxidation times and high temperatures, which can reduce minority carrier lifetimes in silicon wafers through thermal stress, oxygen precipitation or contamination during the high temperature process. The significant thermal budget incurred in forming thermal oxides is not compatible with the trend of reducing manufacturing cost in the photovoltaic industry. Therefore the development of alternative techniques of oxidation at low temperatures is of great significance.

Several low-temperature oxidation processes have been developed, which have resulted in good surface passivation (see Table 1). These include chemical vapour deposition (CVD) processes, such as plasma enhanced CVD (PECVD) [11-13], atmospheric pressure CVD (APCVD) [14, 15] and expanding thermal plasma (ETP) technique [16]. While CVD techniques have demonstrated SRVs less than 100 cm s^{-1} , the reactors used in these deposition systems require a large amount of maintenance and the precursors used to form SiO_2 are both dangerous and expensive.

Alternatively, SiO_2 can be grown by immersing silicon wafers in an oxidizing solution (e.g., nitric acid (HNO_3) [10-12]). Grant *et al.* reported a SRV of 42 cm s^{-1} by growing SiO_2 in 70 % (w/w) HNO_3 followed by a 1000°C anneal in nitrogen and a subsequent forming gas anneal at 400°C [17]. Although the SRV was low, the advantage of a low temperature wet chemical oxidation was mitigated by a slow oxidation rate and the requirement for a high temperature anneal.

Recent developments in the formation of SiO_2 by anodisation have enabled relatively fast oxide growth rates at room temperature. It has been demonstrated after annealing in oxygen and forming gas at 400°C , the anodic SiO_2 formed with DC and AC bias attained a very low SRV of 35 and 15 cm s^{-1} [18], respectively. The light-induced anodisation (LIA), first reported by Cui *et al.* [19], can result in faster oxide growth and increased uniformity. Similarly to [18], once annealed in oxygen and forming gas at 400°C , the LIA SiO_2 passivated wafers achieved comparable effective minority carrier lifetimes (hereafter effective lifetime) to the as grown thermal SiO_2 . In this paper, we investigate the passivation of p-type silicon surfaces by anodic SiO_2 formed by LIA after annealing in oxygen and forming gas at 400°C for 30 min. Photocouductance and quasi steady state photoluminance (QSS-PL) measurements were conducted to determine the effective lifetime and an upper limit to the SRV. Capacitance-voltage (CV) measurements are performed to assess the charge density (Q_{eff}) associated with the anodic oxide and the density of interface states (D_{it}) at the silicon- SiO_2 interface.

Table 1

A summary of the SRV of SiO_2 formed by different techniques.

Ref.	Oxidation technique	Deposition temp, (anneal temp), ambient	SRV (cm s^{-1})
[1]	Thermally-grown	1050°C , (450°C), forming gas	30
[12]	PECVD	350°C , (400°C), forming gas	500-1300
[15]	APCVD	400°C , (400°C), forming gas	1.2×10^5

[16]	Expanding thermal plasma (ETP)	400 °C, (600 °C), forming gas	54
[17]	Chemical oxidation in nitric acid	108 °C, (1100 °C), nitrogen	107
[17]	Chemical oxidation in nitric acid	108 °C, (1100 °C), nitrogen and (400 °C), forming gas	42
[20]	Immersed anodisation (DC bias)	25 °C, (400 °C), O ₂ and forming gas	35
[18]	Immersed anodisation (AC bias)	25 °C, (400 °C), O ₂ and forming gas	15

2. Experimental

2.1. Sample preparation

Anodic SiO₂ films were prepared on alkaline-textured 3–5 Ω cm p-type Czochralski (Cz) silicon ~16 cm² wafers of a thickness of 180 μm and with a POCl₃-diffused emitter sheet resistance of 80 Ω/□. The p-type surfaces of the wafers were planarised by etching in 25% (w/v) sodium hydroxide (NaOH (J.T.Baker)) at 80 °C for 7 min. A layer of thermal SiO₂ of 18 nm thickness on both surfaces was grown by dry oxidation at 950 °C for 18 min in a quartz tube furnace. After oxidation, the p-type surface of the wafers were single-side etched in 1% (w/v) HF for 2 min to remove any native oxide on the surface before LIA SiO₂ formation and annealing.

The LIA SiO₂ growth was performed in 0.5 M H₂SO₄ (BASF VLSI, where trace metal levels are typically less than 100 ppb) for 15 min as described in [19], which resulted in an anodic SiO₂ layer of 23 nm thick. A constant illumination of 180 W m⁻² was provided by an array of 23 W compact fluorescent light bulbs at a distance of 5 cm from the n-type surface of the wafer. The wafers were anodised under constant positive bias of 15 V, which offset the series resistance in the electrochemical circuit and controlled the operating point of the solar cell close to short circuit. After anodisation, the wafers were annealed in a quartz tube furnace at 400 °C. In order to identify the most effective annealing condition to achieve the best surface passivation, the samples were annealed in either oxygen, forming gas or both. Wafers processed in the above mentioned manner were characterized by x-ray photoelectron spectroscopy (XPS) and transmission electron microscopy (TEM) and published in [19].

To perform CV measurements, the thermal SiO₂ was removed from the n-type surface via HF fuming, and 150 nm of aluminium was thermally-evaporated onto the rear surface to enable electrical contact to the silicon wafer. Finally, circular Al contacts with a diameter of 0.70 mm were evaporated on the front surface to complete the metal-oxide-semiconductor (MOS) structures.

2.2. Characterisation

The effective minority carrier lifetime, τ_{eff} , of the wafers were measured after thermal oxidation and after the post anodisation anneal to enable a direct comparison of surface passivation between the thermal SiO₂ and the anodic SiO₂. Photoconductance measurements were performed using a lifetime tester (WCT-120 from Sinton Instruments) under quasi-steady-state illumination and the generalized analysis [21]. Since QSS-PL measurements are not affected by depletion-region modulation [22, 23], accurate τ_{eff} data at low injection levels was acquired. QSS-PL was conducted on a modified Sinton Instruments WCT-120, which enabled simultaneous measurements of the excess conductance, the photoluminescence intensity, and the generation rate [24].

The wafers used for lifetime measurements contained a phosphorus-diffused emitter on one surface, so the measured τ_{eff} contains contributions from bulk recombination, surface recombination and emitter recombination, and can be represented by:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{1}{\tau_{surface}} + \frac{1}{\tau_{emitter}}, \quad (1)$$

where the bulk recombination lifetime τ_{bulk} was measured by a HF passivation method [25], and the emitter recombination lifetime $\tau_{emitter}$ at high injection levels was described by equation (2) [26]:

$$\frac{1}{\tau_{emitter}} = J_{0e} \frac{\Delta n}{qWn_i^2}, \quad (2)$$

where J_{0e} was the emitter dark saturation current, W was the thickness of the wafer, n_i was intrinsic carrier concentration, and Δn was the minority carrier concentration. The surface recombination lifetime was then determined by solving $\tau_{surface}$ in equation (1) and the upper limit of the SRV on the p-type surface can then be calculated by equation (3) with a high level of accuracy [27]. The τ_{eff} and SRV values for LIA anodic SiO₂ reported in this paper are measured/calculated at an injection density of $\Delta n = 10^{15} \text{ cm}^{-3}$.

$$SRV \leq \frac{W}{\tau_{surface}}, \quad (3)$$

Capacitance-voltage measurements were performed at high frequency (1MHz) using a 4284A Precision LCR meter and at low frequency using a 4014B pA meter. From these measurements, Q_{eff} was determined from the flat band voltage of the high frequency curves, while the D_{it} was calculated using the Terman [28] and Castagne [29] methods, with the latter technique being the more accurate.

3. Results and discussion

3.1. Effect of annealing ambient

The effect of annealing ambient was studied to identify the annealing condition that resulted in the most effective surface passivation. Fig. 1 shows the injection-level dependent effective lifetime after annealing wafers in oxygen, forming gas and the combination of the two ambients in different sequences. The figure highlights the significant improvement in surface passivation after annealing. However the improvements varied from one to two orders of magnitude in the effective lifetime between different annealing ambient and varied sequences. The experiment demonstrated that the best passivation was attained by first annealing the LIA SiO₂ in oxygen and then in forming gas at 400 °C for 30 min each, which was consistent with findings reported by Grant *et al.* [20].

The thermal oxidation in dry oxygen stream at 950 °C was used to establish a reference. Fig. 1 shows the anodic SiO₂ with the oxygen and then forming gas anneal attained comparable effective lifetime to the as-grown thermal SiO₂. However the effective lifetime of thermal SiO₂ was further improved after the same annealing process, suggesting the silicon-SiO₂ interface of anodic SiO₂ was more vulnerable to process-induced defects.

Fig. 1. Injection-level dependent effective lifetime of wafers passivated by thermal SiO₂ (TO) and anodic SiO₂ (AO) before and after annealed in either oxygen or forming gas or combinations of the gases.

3.2. Interface quality

To determine the reason for a lower τ_{eff} after annealing with anodic SiO₂ compared to thermally-grown SiO₂, the D_{it} and Q_{eff} were measured by CV, where Q_{eff} represents the combined influence of electrostatic charge and mobile charge in the dielectric. Fig. 2 plots the normalised capacitance as a function of voltage for SiO₂ layers grown by thermal oxidation and LIA. The figure shows that the anodic SiO₂ contained a much lower positive charge ($3.4 \times 10^{11} \text{ cm}^{-2}$) than the thermally-grown SiO₂, as determined by the voltage shift in the measured CV curve. Although the LIA process was performed under DC bias, the resulting Q_{eff} was an order of magnitude lower than oxide formed under DC bias with the immersed anodisation technique [30]. Surprisingly, the Q_{eff} was even lower than oxide anodised under AC bias ($6 \times 10^{11} \text{ cm}^{-2}$), by which a lower Q_{eff} is usually attained [18]. The low Q_{eff} of LIA anodic SiO₂ may be due to the low bias voltage required during anodisation. A low Q_{eff} is advantageous for a dielectric with stored positive charge when applied to a p-type silicon surface, as the SRV is less sensitive to injection level and inversion layer shunting can be mitigated [31].

Fig. 2. Comparison of the measured CV curves of thermal SiO₂ and LIA anodic SiO₂ after oxygen and forming gas anneal at 400 °C for 30 min each.

Fig. 3 shows the D_{it} of the thermal SiO_2 and LIA anodic SiO_2 determined by the Castagne method. During the anneal in oxygen and forming gas, it is hypothesised that hydrogen present in the oxide film passivated recombination-active defects at the silicon- SiO_2 interface, therefore decreased the D_{it} at mid-gap to an average value of about $6 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$. Although the D_{it} measured was an order of magnitude higher than measured for thermal SiO_2 , it was lower than any oxides anodised in an inorganic electrolyte under high DC bias (e.g., 30-500 V). This may result because oxidation under very high bias voltages has been reported to occur at the surface due to cation flow through the growing oxide rather than at the interface [32], therefore the silicon- SiO_2 interface after anodisation was the initial silicon surface, which presented a larger density of interface states. With the LIA technique, however, the low to moderate bias voltage may not have been strong enough to drive the anodic reaction to the surface and therefore anodisation is more likely to have occurred at the silicon- SiO_2 interface where fewer defects are generated. The accumulation of positively charged carriers close to the p-type surface due to light-induced current most likely enhanced the inward movement of the oxidizing agent, such as dissociated oxygen ions (O^-) [33]. As shown in Fig. 4, at the start of anodisation the process was limited by injection of positively-charged carriers. With the increased thickness of the oxide, the resistance of oxidizing agent inward diffusion was increased and the process started to be limited by the supply of oxidizing agent. In doing so, it is proposed that the final silicon- SiO_2 interface was formed at the end of the anodisation process, which resulted in improved interface quality.

Fig. 3. The D_{it} of thermal SiO_2 and LIA anodic SiO_2 after oxygen and forming gas anneal at 400 °C for 30 min each.

Fig. 4. Anodisation current versus time curve of LIA anodic SiO₂ growth showing the different growth regimes.

To accurately measure the SRV of anodic SiO₂ grown by LIA, the bulk lifetime was measured by a HF passivation method [25]. By immersing the wafer in 20% (w/w) HF during a transient photoconductance measurement, a bulk lifetime of 795 μs was measured, which corresponded to a SRV of 62 cm s^{-1} at $\Delta n = 10^{15} \text{ cm}^{-3}$. Similar to the most anodic SiO₂ films, the SRV of the LIA SiO₂ is significantly lower than oxides grown by CVD techniques, which is primarily due to the improved quality of the anodic-grown interface over deposition. This SRV is comparable to the lowest reported SRV of anodic SiO₂ formed under DC bias at the same injection level (65 cm s^{-1} [18]). Further reduction of the SRV may be realised by applying an alternating bias during anodisation, which increases the probability that the defect sites and interface traps of anodic SiO₂ are repaired by driving O⁻ and OH⁻ ions back and forth across the growing oxide film [18, 33].

3.3. Density of anodic SiO₂

Fig. 5 plots the leakage current density for three different SiO₂ films. The red diamonds, blue triangles and black squares represent direct current anodic SiO₂ [20], LIA SiO₂ and thermal SiO₂ respectively. From the figure, it is evident that the LIA SiO₂ has the lowest leakage current density over the voltage range examined. Although the LIA SiO₂ film has the highest oxide thickness, it is not expected that such a large difference in leakage current density would result purely from the different thickness. Consequently we attribute the large differences in leakage current density to physical differences in the films. The leakage current density demonstrated by the LIA SiO₂ is also lower than measured for anodic SiO₂ grown in nitric acid either at much higher grown temperature (113 °C) [34] or with high annealing temperature (600 °C) [35].

From Fig. 5, it is surprising to see that the thermal SiO₂ has a relatively high leakage current when compared to the anodic SiO₂ films (DC and LIA), even though its measured D_{it} was the lowest of the three films. Therefore, even though the LIA anodic SiO₂ film exhibits higher surface recombination due to a higher D_{it} and lower Q_{eff} , the film appears to be quite dense and with relatively few defects, as evident by the much lower leakage current densities. This result is also consistent with the ellipsometry measurements, which demonstrate that the LIA SiO₂ films have a higher refractive index of 1.49 than thermal SiO₂. The apparent zero-current shift in the I-V curve of the LIA SiO₂ is most likely related to the trapped charges at the silicon/anodic SiO₂ interface. When the voltage is zero, current still flows because the trapped charge acts like a negative offset voltage, thus until a voltage opposing the trapped charge is reached, the current doesn't achieve the minimum current. Mobile

charges in the oxide film is hypothesised to be another cause of the shift to negative voltage bias, which has been observed in an oxygen-plasma oxidised AlO_x film [36]. Another possible explanation could result from the accuracy of the 4140 pA meter at such low leakage current values. It is possible that a very small offset current could exist in the system, which may impact the zero current along the voltage axis and cause a large ‘apparent’ voltage shift. This however still implies that our leakage current for LIA SiO_2 is still much lower than that for thermal and DC anodic SiO_2 .

Fig. 5. I - V curves for the MOS diode with thermal SiO_2 , DC anodic SiO_2 and LIA anodic SiO_2 being the intervening dielectric.

The high growth rate of the LIA SiO_2 is also advantageous. Fig. 6 shows the thickness of the LIA SiO_2 films as a function of the anodisation time under 15 V bias voltage and 180 W m^{-2} illumination. An LIA SiO_2 layer 23 nm thick was formed at 25°C after 15 min anodisation, which contrasts to 3 hours [20] and 4 hours [35] for immersion anodisation in the HNO_3 . The growth rate can be further improved by way of increasing light intensity or bias voltage [19].

Fig. 6. Thickness of LIA SiO_2 layers as a function of the anodisation time. Error bars are showing the standard derivation of five points measured on each wafer.

Featuring excellent low leakage current and high growth rate, the LIA SiO₂ films could potentially find applications in interdigitated back contact (IBC) solar cells, where it is imperative to isolate p- and n-type contacts from one another, in order to inhibit shunting and maintain high solar cell efficiencies. The low leakage current also suggests that they may provide an effective barrier for PID.

4. Conclusions

This paper reports the formation of anodic SiO₂ by LIA at high growth rate and with demonstrated effective surface passivation on p-type crystalline silicon surfaces. The influence of the annealing ambient and the annealing sequence were investigated, showing annealing in oxygen and forming gas at 400 °C more effectively decreased the D_{it} presumably by passivating recombination-active defects at the silicon-SiO₂ interface. The lowest D_{it} attained was $5.5 \times 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$, comparable to the literature but processed at room temperature and at a much lower bias voltage. The anodic SiO₂ possessed an ultra-low average Q_{eff} at $+3.4 \times 10^{11} \text{ cm}^{-2}$, which would be advantageous in reducing the inversion layer shunting when localised metal contacts are formed on p-type surfaces. Additionally, the LIA anodic SiO₂ had a lower leakage current density (3.5×10^{-10} and $1.6 \times 10^{-9} \text{ A cm}^{-2}$ at 1 and -1 V, respectively) compared to anodic SiO₂ formed by other techniques, which make LIA anodic SiO₂ films a promising insulation dielectric for IBC solar cells. It may also find applications in metal plating and potential induced degradation prevention when integrated in the antireflection coating of silicon solar cells, whilst providing a new alternative for contact passivation.

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