A Radiation-Hard Dual-Channel 12-bit 40 MS/s ADC Prototype for the ATLAS Liquid Argon Calorimeter Readout Electronics Upgrade at the CERN LHC

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Abstract

The readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN Large Hadron Collider requires a radiation-hard ADC. The design of a radiation-hard dual-channel 12-bit 40 MS/s pipeline ADC for this use is presented. The design consists of two pipeline A/D channels each with four Multiplying Digital-to-Analog Converters followed by 8-bit Successive-Approximation-Register analog-to-digital converters. The custom design, fabricated in a commercial 130 nm CMOS process, shows a performance of 67.9 dB SNDR at 10 MHz for a single channel at 40 MS/s, with a latency of 87.5 ns (to first bit read out), while its total power consumption is 50 mW/channel. The chip uses two power supply voltages: 1.2 and 2.5 V. The sensitivity to single event effects during irradiation is measured and determined to meet the system requirements.

Keywords: Calorimeters, Radiation-hard electronics, Front-end electronics for detector readout, ADC, Radiation-tolerant

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1. Introduction

This article describes the design and performance of a radiation-hard dual channel 40 MS/s pipeline ADC prototype. A future version of this ADC is intended for the upgraded trigger electronics in the ATLAS Liquid Argon (LAr) Calorimeter readout. The current prototype is used to establish the analog performance of the four 1.5-bit pipeline stages and the 8-bit Successive-Approximation-Register (SAR) ADC stage, and to study the radiation tolerance of the ADC design. This work is an extension of the ADC design in [1]. There, the performance of the four 1.5-bit pipeline stages was presented, verifying the precision of the design as well of as the radiation hardness of the pipeline stages. This article introduces the SAR ADC stage, its integration with the pipeline stages, and a measurement of the sensitivity of the ADC to single event upsets (SEU) during irradiation.

The Large Hadron Collider (LHC) [2] at CERN is a proton-proton collider designed to operate at center-of-mass energies of 7–14 TeV. The LHC began circulating 6.5 TeV beams in 2015 and is expected to operate at approximately this energy for the rest of the decade. The ATLAS detector [3] is a multi-purpose apparatus built to observe the decays of particles produced by the high energy collisions at the LHC. The position and energy of electrons and photons from these decays are measured by the electromagnetic calorimeter system. This system consists of three calorimeters (a barrel and two end-caps in separate cryostats). These sampling calorimeters are read out by an analog and digital electronics chain. To precisely record the large dynamic range signals produced by the calorimeters and to limit noise, part of the electronic chain (the front-end) is located on the detector [4].

Providing data to the on-line event selection (trigger system) is an important function of the LAr calorimeters. Electron and photon triggers are critical to the ATLAS physics program. The acceptance rate of these triggers will be affected by the planned LHC upgrades. Upgrades to the LHC are scheduled to occur in two stages, starting with Phase 1 in 2019-2020 and then for the High Luminosity LHC (HL-LHC) in 2024-2026 [5]. These upgrades will increase the instantaneous luminosities from the nominal value ($10^{34} \text{ cm}^{-2}\text{s}^{-1}$) to three times that for the data collected in 2021-2023 (after Phase 1) [6]. For electron and photon triggers, which rely on the LAr calorimeter data, higher instantaneous luminosities would require increased energy thresholds. To avoid raising the thresholds additional data can be provided by LAr calorimeters to the trigger system. This allows the use of

38 more efficient algorithms to reduce background events [6].

39 Currently, the existing front-end electronics limit the granularity, band-
 40 width and latency of the data transmitted to the lowest level of the trigger
 41 system. With the addition of new interface electronics between the LAr
 42 calorimeters and trigger system higher granularity data can be provided at
 43 the bunch crossing rate of 40 MHz. This will take the form of a LAr Trigger
 44 Digitizer Board (LTDB), illustrated on the bottom left of Figure 1 and to be
 45 installed as part of the Phase 1 upgrade. The design and strategy of the LAr
 46 calorimeter trigger electronics upgrade is described in greater detail in [6].
 47 A suitable ADC is an important requirement of this upgrade. Though to be
 48 installed as part of the Phase 1 upgrade, this ADC is designed to operate
 49 throughout the HL-LHC run.

Figure 1: Block diagram for the proposed ATLAS Phase-I electronics upgrade [6]. The analog signals enter the system on the upper left, and are passed to the trigger system and DAQ system. The position of ADC is indicated in the lower left box (LTDB), digitizing the signals for the trigger system.

2. ADC Architecture

2.1. ADC Specifications

This ADC is designed to digitize the analog signals from the LAr calorimeters before they are transmitted to the trigger system. The raw calorimeter signal is a triangular pulse about 500 ns long. This signal is passed through a preamplifier and is then subject to a fast bipolar $CR - (RC)^2$ shaping function with $\tau = RC = 20$ ns. In the precision readout of the detector these shaped signals are further amplified with a gain of 1, 10 or 100 to reduce the dynamic range requirements. However, for the trigger readout four channels are summed before shaping and no gain is applied. In the upgraded system these shaped signals will be sent to new Layer Sum Boards [6], which will combine the output of the shapers for each of the four calorimeter layers. In each layer either four or eight channels will be combined into one signal to be digitized. This will provide higher granularity readout when compared to the existing system of “trigger towers.” The “trigger towers” combine additional cells laterally, as well as the four layers, into a single tower.

The ADC for Phase 1 must meet the following specifications:

- The calorimeter signals must be continuously sampled and digitized at (minimally) a frequency of 40 MHz.
- The ADC power must be less than 145 mW.
- The latency must be less than 200 ns.
- It must be radiation tolerant up to 75 kRad Total Ionizing Dose (TID) and tested for SEU with a total fluence of $3.8 \times 10^{12} h/cm^2$.
- The energy measurement requires a dynamic range of approximately 12 bits to digitize energies from 32 MeV to 102 GeV for the front layer trigger cells and from 125 MeV to 400 GeV in the middle layer trigger cells [6].

This combination of speed, precision, low power, and particularly radiation hardness is not readily available commercially. The following sections describe a chip that meets these specifications.

2.2. Radiation Tolerance

Though designed for Phase 1, the ADC is expected to continue to perform reliably throughout the operation of the HL-LHC. For the expected total integrated luminosity of 3000 fb^{-1} the LAr electronics are required to be radiation tolerant to a TID of 75 kRad, and tested for Single Event Effects (SEE) with a total fluence of $3.8 \times 10^{12} \text{ h/cm}^2$ [5]. The radiation at the LAr electronics comes predominantly from secondary particles produced by interactions of primary particles with the detector elements. The most significant contribution to the flux in the LAr electronics are photons and neutrons. Charged hadrons (mainly protons and pions) are a smaller contribution.

A commercial 130 nm CMOS process was selected for this ADC. The rated supply voltage of thin (thick)-oxide 130 nm devices is 1.2 V (2.5 V). The 130 nm CMOS process has been demonstrated for both thin-oxide and thick-oxide MOS devices to be radiation hard to a few tens of MRads [7, 8]. It was noted [9] that thin-oxide devices are more radiation tolerant than thick-oxide devices. However, a previous design [1] of a multiplying digital-to-analog converter (MDAC) using thick-oxide devices in this technology showed that standard hardness-by-design layout techniques were sufficient to achieve the necessary radiation tolerance. The thick-oxide devices allow for an input signal swing of the ADC of 2.4 V_{p-p} differential, relaxing the noise requirements in the ADC.

2.3. Prototype Implementation

The goals of the current prototype are to test the performance of the complete ADC (extended from [1] with the addition of an 8-bit SAR backend), verify the on-chip, digital mismatch calibration and study the radiation tolerance of the ADC. The prototype's architecture, shown in Figure 2, consists of two identical 12-bit 40 MS/s pipeline and SAR ADC channels. In 130 nm CMOS capacitor matching is not guaranteed to the precision required for a 12-bit ADC. The pipeline architecture allows for a calibration to correct gain errors due to the capacitor mismatch. The two ADC channels are fed with V_{in1} and V_{in2} respectively.

Each of the two ADC channels in the current prototype consist of four MDAC stages with a gain of two each. Each MDAC stage resolves one bit, followed by a times two residue amplification. The three possible output codes ("1.5 bits") allow for the digital error correction. The analog residue of the fourth and final MDAC stage needs to be further resolved to 8-bit accuracy to determine the final 12-bit ADC word. This analog residue is fed

Figure 2: Prototype architecture.

117 to the 8-bit SAR to determine the eight least significant bits. In the current
 118 prototype, the stage-1 MDAC is nominally 12-bit accurate, identical to the
 119 MDAC in [1]. To reduce power consumption the following three MDACs
 120 are scaled. The scaling is achieved by reducing the silicon size and therefore
 121 the power used in these MDACs. The main building block of the MDACs
 122 is the Operational Transconductance Amplifier (OTA). The OTA for stages
 123 2-4 requires less than the 12-bit precision of the first stage. Therefore, the
 124 open loop gain can be lower and the sampling capacitor size can be smaller,
 125 reducing the power consumed. The implementation details of the ADC are
 126 further explained in the following sections.

127 2.3.1. MDAC and OTA Implementation

128 Figure 3 shows the architecture of the 1.5-bit MDAC stage and OTA
 129 used in the pipeline ADC [10]. This architecture was described in detail in
 130 a previous paper [1]. The MDAC consists of a flip-around architecture with
 131 the input V_{in} sampled onto the sampling capacitors C_s and the flip-around
 132 capacitors C_f , during the sampling phase ϕ_s . Nominally, C_s and C_f are
 133 equal. At the beginning of the hold phase ϕ_h , depending on the subADC

Figure 3: 1.5b MDAC stage (subADC not shown); ϕ_s/ϕ_h - sample/hold phase; ϕ_{se}/ϕ_{he} - advanced version of ϕ_s/ϕ_h ; V_{CM} - common-mode voltage; V_{ref} - reference voltage; D - subADC decision.

134 decision D , the reference V_{ref} is appropriately connected to the capacitors,
 135 thus performing the required MDAC operation given by

$$V_{out} = 2V_{in} - DV_{ref} \quad (1)$$

136 where $D = 0, \pm 1$ is the subADC decision. The subADC (not shown) consists
 137 of a flash comparator and an input sampling network. The OTA consists of
 138 a single stage, gain-boosted, folded cascode amplifier with an NMOS input
 139 pair. The OTA is designed for a DC gain of 80 dB (first stage) and a UGB of
 140 450 MHz, thus providing enough margin for the targeted 12-bit performance
 141 at 40 MS/s.

142 2.3.2. SAR Implementation

143 The eight least significant bits of the ADC are resolved using a SAR. A
 144 synchronous SAR design was chosen for simplicity and the relatively moder-
 145 ate speed and resolution requirements (8-bit and 40 MS/s). Figure 4 shows
 146 the simplified block diagram of the 8-bit SAR, with the digital logic not
 147 shown. A single-ended version is shown for simplicity, whereas the actual
 148 implementation is fully differential.

149 The selection of the total SAR input capacitance is a compromise be-
 150 tween the radiation tolerance, noise and mismatch. The required radiation
 151 tolerance necessitates the use of larger unit capacitor sizes than dictated by

Figure 4: The SAR architecture block diagram. A single-ended version is shown for clarity, whereas the actual implementation is fully differential.

the 8-bit noise and matching requirements. The SAR uses a unit capacitor size of 59.6 fF. This capacitor size is smallest MiM (Metal-insulator-Metal) capacitor with best mismatch in the technology used. To reduce the total capacitance of the SAR with the chosen unit capacitor size, the SAR capacitor array is segmented, as shown in Figure 4. The first four largest capacitors are binary scaled with a total capacitance of $15C$, while the final three capacitors have the same unit capacitance C . To enable binary successive approximation, the final three capacitors are fed with the scaled reference voltages of $(\pm V_{ref}/2, \pm V_{ref}/4, \pm V_{ref}/8)$ obtained through a resistive ladder.

During the sampling phase, the residue from the stage four MDAC is sampled into the capacitor array. The switches $S1$ to $S7$ are in the “IN” position (see Figure 4). The SAR conversion process starts with turning switch S off and switches $S1$ to $S7$ to the position “P,” when all the capacitors are pulled to V_{CM} (0.6 V) and the most significant bit (D_1) is resolved. Sequentially, as a result of the comparison, switches $S1$ to $S7$ are moved to position “SO” based on the decisions D_i to perform the successive approximation operation by adding or subtracting charge from input signal.

The MDAC stages, implemented using thick-oxide MOS devices, operate

Figure 5: Detail of switches for the voltage shift network, necessary at the MDAC-SAR interface when the SAR (1.2 V supply) samples the input MDAC signal (2.5 V supply).

170 from a supply voltage of 2.5 V and a common-mode of 1.25 V. The 8-bit
 171 SAR is implemented using thin-oxide MOS devices in a supply voltage of
 172 1.2 V with a common-mode of 0.6 V for low-power operation (SAR power
 173 consumption is $\approx fCV_{DD}^2$ where $V_{DD} = 1.2$ V). This realizes the SAR digital
 174 logic using available standard thin-oxide cells. As a result of the different
 175 voltage domains of the MDACs and the SAR, a level shift network is neces-
 176 sary at the MDAC-SAR interface when the SAR samples the input signal.
 177 Figure 5 shows the detailed implementation of the DC level-shift network
 178 incorporated in the switches $S1$ to $S7$ that accomplishes this operation.

179 The SAR input sampling phase is simultaneous with the hold phase of
 180 MDAC4. While the WR signal is active, switches $SW4$ and $SW5$ (in Fig-
 181 ure 5) sample the input signal onto one plate of the capacitors. Meanwhile,
 182 switches $SW1 - 3$ short the other plate to 1.25 V, the common-mode voltage

183 of the MDACs. During the sampling time the thin-oxide switches $SW13 - 16$
 184 are protected from any over-voltage by switches $SW8$ and $SW12$. After the
 185 sampling phase the left plate of the capacitors is pulled down to 0.6 V us-
 186 ing switches $SW9 - 10$ (while the RD signal is active). This accomplishes
 187 the common-mode translation from 1.25 V to 0.6 V. At the same time, the
 188 comparator compares the voltage on its CAP inputs and produces the SAR
 189 digital output for a given bit. The result is applied in the next 640 MHz clock
 190 tick by adding or subtracting the reference voltage from the sampled signal.
 191 The SAR unit is operated in pipeline mode with the MDACs. The com-
 192 plete SAR operation requires 12.5 ns (one half of one sampling period). The
 193 SAR digital control of switches and outputs is implemented using standard
 194 1.2 V logic, with standard D flip-flops (the primary state machine memory
 195 elements) clocked at 640 MHz.

196 *2.3.3. Digital Data Processing Unit and Digital Gain Calibration*

197 Digital signals from the MDACs and the SAR are processed by the digital
 198 data processing unit (DDPU). The DDPU aligns the data in time, performs
 199 the digital correction and forms the A/D result. In Figure 6 the time struc-
 200 ture of the digitization is shown, with a latency (to first bit read out) of
 201 87.5 ns. The digital output of each ADC pipeline stage is produced sequen-
 202 tially using both edges of the sampling clock. In order to form the final ADC
 203 word such an output must be aligned: this is done by registering the data in
 204 the DDPU and adding the correct number of registers before summing.

205 The most important function of the DDPU is the MDAC digital gain
 206 correction. Foreground digital calibration is performed to correct for gain
 207 errors due to capacitor mismatch [11], exploiting the redundancy offered by
 208 the three possible codes produced to resolve one bit. Figure 7 shows the
 209 residue output V_{res} of the stage 1 MDAC and the reconstructed output D_{out} ,
 210 as a function of the input V_{in} , for an ideal MDAC and for an MDAC with
 211 gain error. Gain errors due to capacitor mismatch give rise to code jumps
 212 in the reconstructed output, as shown by Δ in Figure 7. The calibration
 213 algorithm consists of measuring the MDAC code jumps Δ by subsequent
 214 ADC stages and removing them digitally from the reconstructed digital out-
 215 put D_{out} . The calibration procedure starts with the last MDAC stage (the
 216 stage 4 MDAC in this prototype) and moves backward to calibrate the stage
 217 1 MDAC. An on-chip control register is used to put the ADC in calibration
 218 mode. Once determined, the eight 12-bit calibration constants are stored in
 219 a triple-redundant buffer by the chip calibration and control system.

Figure 6: DDPU block diagram. The DDPU applies the calibration to the digital output of each MDAC and forms the final ADC word.

Figure 7: MDAC residue characteristic (left). Reconstructed output (right); V_{ref} - reference voltage; V_{res} - residue voltage; D - subADC decision; D_{out} - reconstructed output.

Figure 8: Clock architecture block diagram.

220 The final ADC word is formed with the 3-way adder when the correspond-
221 ing SAR output is available. This 12-bit word is sent off-chip in serial form
222 at 640 MHz. In total, 16-bits of serial data are sent, usually with four bits
223 set to zero. The DDPU can also send out the uncorrected digital data from
224 each MDAC and SAR, using all 16-bits. The DDPU unit is implemented
225 using fully synthesized logic using standard CERN scripts for commercial
226 130 nm digital libraries with Verilog input. The DDPU operates at 80 MHz
227 and consumes ~ 3 mW of power at 1.2 V.

2.3.4. Clock Generator Implementation

228 A 640 MHz sinusoidal clock is fed into the chip and divided down to
229 generate the required 40 MHz clock phases, while a separate 40 MHz clock
230 provides the frame. The clock signal and time-critical control signals are
231 produced inside the clock generator unit (Figure 8). The reliable transmission
232 of serialized output requires either a precise and stable clock or a Phase Lock
233 Loop (PLL). A precise clock is also critical at the interface between MDAC
234 stages (operating at 40 MHz) and the SAR stage (operating at 640 MHz). As
235 an alternative to operating an on-chip PLL in a radiation environment, this
236 ADC tests the on-board distribution of 40 MHz and 640 MHz clocks. Both
237 clock signals are distributed using the scalable low-voltage signaling (SLVS)
238 protocol [12]. The timing information is expected to be on the positive edge
239 of the 640 MHz signal; therefore, the receiver of this signal must meet the
240 jitter requirements for a 12-bit ADC (~ 1 ps). This implementation does
241 not expect the clock signals to be synchronized, and provides the ability to
242 adjust the clock relationship using a programmable delay (up to ~ 3 ns for
243 the 640 MHz clock).

245 The 40 MHz clock provides the frame for the sampling. The edge of the
 246 frame is detected by the 640 MHz clock, and the information passed to a
 247 16-bit shift register. This arrangement allows the straightforward generation
 248 of the ADC sampling phases ϕ_1 and ϕ_2 with a simple RS flip-flop. The ability
 249 to adjust the start of the ϕ_1 and ϕ_2 signals by up to eight 640 MHz clock
 250 steps using a programmable delay is provided. The same shift register also
 251 distributes the timing critical signals for loading the serializer and starting
 252 the SAR operation, and this location contains the fan-out of the fast clocks
 253 inside the ADC (640 MHz for SAR operation and 640 MHz for serialization).

254 2.3.5. Calibration and System Control

255 The calibration and system control block (CSC) provides the slow control
 256 for all systems on the chip. The CSC uses a three wire serial interface (5 MHz
 257 clock, $data_{in}$ and $frame_{in}$) to write to the chip registers and a two wire serial
 258 interface ($data_{out}$, $frame_{out}$) to read them back. The CSC communicates with
 259 the DDPUs inside the chip using the same serial protocol. The control
 260 signals are retimed internally and the destination address within the DDPUs is
 261 added to the external protocol. Output data from the DDPUs are multiplexed
 262 to two wires, which allows the loading of all calibration parameters and
 263 internal MDAC signals needed to perform the calibration. The CSC unit
 264 contains the triple redundant memory (to protect against SEU) for the chip
 265 configuration and is a fully synthesized block using the 1.2 V standard library.

266 2.3.6. Serializer

267 The serializer unit (Figure 9) consists of a parallel register and a shift
 268 register. With each 640 MHz clock signal, the data are written into a parallel
 269 register. In normal operation the unit can send out calibrated ADC data,
 270 or alternatively a test pattern or uncorrected data. At the end of the shift
 271 operation the parallel register data are loaded into the serial register and
 272 shifted outside the chip. The start of the new shift operation is marked by
 273 the frame signal, which is also sent with the data. A 320 MHz clock signal
 274 is sent in parallel with the serial ADC data. The clock signal is produced
 275 locally in the serializer by dividing the 640 MHz clock. Each edge of the
 276 320 MHz clock signal is used to strobe the data in the off-chip de-serializer
 277 unit. The serializer unit is implemented using the standard 1.2 V library.
 278 The ADC data, clock signal and the frame are driven outside the chip using
 279 SLVS drivers designed at CERN [13]. To ensure radiation hardness triple
 280 redundant logic is used in the following manner: If the D-flip flops are part

Figure 9: Serializer block diagram showing the parallel and shift registers.

281 of the state machine, or if they store the calibration or other slow control
 282 bits, then they are tripled and the result is generated by voting. D-flip flops
 283 where the outputs are recomputed from scratch by up to two free running
 284 clock cycles are not triple redundant.

285 3. Measurement Results

286 Figure 10 shows a die photograph of the 2-channel ADC prototype. The
 287 chip occupies 6 mm². To characterize the dynamic performance of the ADC,
 288 an input sinusoidal signal is filtered to remove harmonic components and
 289 fed to the ADC input. To allow for flexibility in testing, the signal can be
 290 sent either to the ADC input, or bypassing the MDACs directly to the SAR
 291 ADC input. This feature allows the testing of the SAR stage as a separate
 292 8-bit ADC. The digitized output can either be sent directly off-chip, or the
 293 calibration can be applied. The digital outputs from the prototype chip are
 294 collected by an FPGA. Thirty chips were packaged and functional tests were
 295 performed with a socketed test board, with a yield of approximately 90%.
 296 The socketed board limited the precision of the measurements. Therefore, to
 297 determine ADC performance, two of the functional chips were soldered onto
 298 a precision test board.

299 3.1. ADC Performance

300 Both ADC channels of the two chips mounted on the precision test boards
 301 were characterized. The 8-bit SAR ADC was first characterized indepen-

Figure 10: ADC die photograph.

302 dently of the MDACs. This was a critical test of the SAR and a major goal in
 303 designing this chip. The static performance of the ADC was measured by the
 304 sine-wave histogram method [14]. Figures 11 and 12 show the typical static
 305 performance of one 8-bit ADC channel at 40 MS/s. The integral nonlinearity
 306 (INL) is $+0.45/-0.52 \text{ LSB}_8$, where LSB_8 refers to the Least Significant Bit
 307 (LSB) of 8-bits. The differential nonlinearity (DNL) is $+0.58/-0.41 \text{ LSB}_8$.
 308 Figure 13 shows the output fast Fourier transform (FFT) of a 10 MHz input
 309 sine-wave. The effective number of bits (ENOB) at 10 MHz is 7.7-bits and
 310 the spurious-free dynamic range (SFDR) is 60.3 dB. This performance was
 311 typical for all chips that passed the functionally tests, as the socketed board
 312 did not limit the precision of these tests.

313 The SAR stage is used to calibrate the MDAC stages, and the perfor-
 314 mance of the full 12-bit ADC is measured. Figures 14 and 15 show the static
 315 performance of one 12-bit ADC channel at 40 MS/s. Similar performance is
 316 observed on both channels for both chips and crosstalk between channels is
 317 not observed. The INL is $+1.12/-1.44 \text{ LSB}_{12}$ and the DNL is $+1.33, -0.62$
 318 LSB_{12} . The typical size of the calibration correction for each MDAC is 2–7%.
 319 Figure 16 shows the output FFT of a 10 MHz input sine-wave after digital
 320 calibration. The ENOB at 10 MHz for the calibrated channel is 11.0-bits,
 321 calculated from the signal to noise and distortion ratio (SINAD) of 67.9 dB,
 322 and the SFDR is 79.4 dB. The measurements are repeated at input signal

Figure 11: 8-bit SAR sub-ADC INL at 40 MS/s (*Chip 1*).

Figure 12: 8-bit SAR sub-ADC DNL at 40 MS/s (*Chip 1*).

Figure 13: 8-bit SAR sub-ADC FFT for $f_{in} = 10$ MHz (*Chip 1*).

323 frequencies of 200 kHz and 18 MHz, verifying the expected performance ob-
 324 served in [1]. The total analog power consumption of the chip is 50 mW per
 325 channel.

326 The dynamic performance can be compared to the expected ~ 11.5 ENOB
 327 performance of the MDACs [1]. The decrease is due to two challenges en-
 328 countered with the design of the chip. The first is related to the architecture
 329 of the chip. The four MDACs in pipeline mode operating at 40 MHz are
 330 followed by the SAR operating at 640 MHz (this frequency choice was influ-
 331 enced by the low-jitter 640 MHz clock required for serialization). In order
 332 to fit the nine 640 MHz clock cycles (eight for the SAR operations plus one
 333 for the common mode voltage change) into exactly one half of a 40 MHz
 334 cycle both edges of the 640 MHz clock are used. This requires a well-defined
 335 duty cycle for the 640 MHz clock with respect to the 40 MHz clock. This
 336 chip does not have reconditioning hardware to restore the duty cycle during
 337 operation. This causes the MDACs and SAR to no longer be perfectly in
 338 phase. The results are spurious codes where the MDAC and SAR output
 339 are not synchronized, degrading the performance. This was confirmed with
 340 transistor-level simulations. Clock adjustments were made for individual
 341 chips which reduced the number of spurious codes. In the next generation of
 342 this chip additional hardware has been proposed to recondition the fast clock
 343 duty cycle, as well as hardware to restore the proper relationship between
 344 the slow and fast clocks at the point of use. Alternatively, a system using
 345 only one edge of the fast clock could be used.

346 The second challenge was connected to the design of reference voltage
 347 drivers. Three reference voltages are necessary ($V_{ref}, V_{ref}/4, V_{ref}^{SAR}$). In one
 348 case ($V_{ref}/4$) the open-loop gain of the amplifiers controlling the switched
 349 drivers was insufficient. The resulting voltage source did not supply enough
 350 charge to its load. This was confirmed in transistor-level simulations. An
 351 external reference voltage was provided during the testing, however the op-
 352 tion to completely disable the internal reference voltage was not included in
 353 the design. A solution has been proposed which corrects the open-loop gain,
 354 and may be implemented in the next generation of this chip.

355 3.2. Irradiation

356 The goals of the irradiation testing were to measure the SEE cross section
 357 and to test the radiation tolerance of the SAR ADC (the insensitivity to large
 358 TID of the high precision, MDAC stages was measured in [1]). Five chips
 359 were taken to the Massachusetts General Hospital Francis H. Burr Proton

Figure 14: Full ADC INL at 40 MS/s (*Chip 1*): after calibration.

Figure 15: Full ADC DNL at 40 MS/s (*Chip 1*): after calibration.

Figure 16: Full ADC FFT for $f_{in} = 10$ MHz (*Chip 1*): after calibration.

Figure 17: Test board for irradiation. The length of the board is ~ 30 cm in order to separate the active elements from the ADC under test. The active elements are protected by lead shielding during testing.

Therapy Center. These chips were selected using a socketed board to verify their functionality, and were then mounted on a specialized board designed to allow the readout of the chip during the irradiation. As shown in Figure 17, the chip was placed at one end of the ~ 30 cm long board, while the other active elements, including the FPGA, were placed at the other end. The high radiation flux in the ATLAS detector was replicated by irradiating four of the chips using the 227 MeV proton beam. During the irradiation, the active elements not under test were protected with lead shielding. This board was powered and the current drawn by the chip was monitored. A clock signal was provided, and a pure sine-wave signal was applied to the input of the ADC. The board limited the precision of the measurements to approximately 10 ENOB. The limitation prevented the testing of the full 12-bit resolution. However, previous radiation testing of the MDAC stages established that doses as large as 10 MRad did not measurably degrade the MDAC precision [1].

The performance of the chip over a large TID was measured by irradiating two chips, one to 1 MRad and the other to 2 MRad. During the irradiation, the ENOB of two of the chips was measured every five seconds, while the calibration was performed every 120 seconds. The limited precision was sufficient to determine the 8-bit SAR ADC sensitivity to TID and the SEE cross section. The limited precision also enters the measurement through the calibration. Since the calibration constants are measured with this board, they have a reduced precision as well. This resulted in fluctuations in the ENOB after each new calibration was applied, as observed in Figure 18. The

Figure 18: ENOB monitored during irradiation. The fluxuations in the ENOB are expected and caused by rerunning the calibration procedure several times during the irradiation, as would be done in the use of the device at the ATLAS experiment. Note that on the specialized irradiation board the ENOB is limited to approximately 10. 1100 s corresponds to a dose of 2 MRad, or 75 kRad (the TID specification) in less than 50 s.

384 test demonstrates that the ADC is functioning well after irradiation with
 385 up to 2 MRad with no sign of failures and or large degradation of ENOB
 386 performance: in future testing it may be possible to improve the precision of
 387 the test board. Table 1 lists the dose for the two chips and the performance
 388 measurements before the start of the irradiation and immediately afterwards,
 389 confirming the insensitivity of the 8-bit SAR ADC to TID. The calibration
 390 constants varied by 1 – 2%.

391 Two additional chips were irradiated to measure the SEE cross section.
 392 In this test the sine-wave signal was removed. Outputs within a window
 393 around the pedestal value were removed by a filter applied in the FPGA.
 394 In this way single-event effects could be observed as the appearance of a

Table 1: Measurements of ADC performance before and immediately after irradiation in a 227 MeV proton beam at $f_{in} = 10$ MHz. The change in the ENOB is within the measurement errors of the testing setup.

Chip No.	Dose [MRad]	SNDR [dBc]		SFDR [dBc]		ENOB	
		Pre/Post-Irradiation		Pre/Post-Irradiation		Pre/Post-Irradiation	
1	2	62.43 / 61.05		67.27 / 70.06		10.08 / 9.85	
2	1	63.54 / 62.36		70.92 / 72.98		10.26 / 10.10	

digital output which was outside the filter window, with very little dead time. Additionally, spurious codes (caused by the clock duty cycle issue) which had been observed before irradiation were masked offline.

Table 2 lists the dose and cross section measurements for the two chips. There are three types of SEE observed. The first is a single-event-function-interrupt (SEFI), in which the ADC ceases to operate normally. When detected (constant ADC output is observed) an external reset returns the ADC to normal operation. This is not equivalent to a latchup: restoring operation after a latchup would require power cycling the ADC, therefore it can be concluded that latchup events were not observed. The next is a single-event-upset (SEU), which results in a transient, erroneous code. This can affect either the analog or digital portion of the chip. When the analog signal path is affected the errors can be observed as a distribution around the pedestal value, effectively reducing the resolution of the ADC. As a result of the binary scaling of the capacitors in the SAR, the sensitivity to upsets drops quickly with bit significance. That is, the SEU cross section, in this case, decreases as the magnitude of the induced error in the number of ADC counts increases. If the errors result from the digital portion of the chip (bit-flips) then the errors are typically large deviations from the pedestal value. The total SEE is the sum of these errors. In determining the SEE cross section we exclude the analog errors, as they are primarily a resolution effect, but also indicate the value obtained if such errors were to be included.

4. Conclusion

The design of a radiation-hard dual-channel 12-bit 40 MS/s Pipeline ADC test chip was presented, an important step in the development of an ADC for use in the readout electronics upgrade for the ATLAS Liquid Argon Calorimeters at the CERN LHC. The ADC was confirmed to meet the analog-to-

Table 2: Measurements of ADC SEE performance in a 227 MeV proton beam.

Chip No.	Rate [10^8 proton/cm ² /s]	Dose [kRad]	SEFI	SEU (analog)	SEU (digital)	SEE	Cross section (w/analog errors) [10^{-12} cm ²]
3	19.0	101	0	8	1	9	0.6 (5.7 ± 1.9)
3	76.0	283	0	41	2	43	0.6 (9.8 ± 1.5)
4	18.6	203	1	10	0	11	0.3 (3.5 ± 1.1)

digital conversion performance criteria with 11.0 ENOB and 67.9 dB SNDR at 10 MHz at 40 MS/s, with a latency of 87.5 ns (to first bit read out), while its total power consumption is 50 mW/channel. The new SAR ADC was tested and found to be robust to total dose up to 2 MRad. The SEE cross section was measured to be less than 10^{-12} cm². Several challenges were encountered, specifically the design of the clock conditioning and the reference voltage drivers. In future designs a PLL may be used to ensure the reliable transmission of serialized output, while for the reference voltage a solution correcting the open-loop gain has been investigated.

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