Study of built-in amplifier performance on HV-CMOS sensor for the ATLAS Phase-II Strip Tracker Upgrade

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Abstract

This paper focuses on the performance of analog readout electronics (built-in amplifier) integrated on the high-voltage (HV) CMOS silicon sensor chip, as

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well as its radiation hardness. Since the total collected charge from minimum ionizing particle (MIP) for the CMOS sensor is ten times lower than for a conventional planar sensor, it is crucial to integrate a low noise built-in amplifier on the sensor chip to improve the signal to noise ratio of the system. As part of the investigation for the ATLAS strip detector upgrade, a test chip that comprises several pixel arrays with different geometry, as well as standalone built-in amplifiers and built-in amplifiers in pixel arrays has been fabricated in a $0.35\ \mu\text{m}$ high-voltage CMOS process. Measurements of the gain and the noise of both the standalone amplifiers and built-in amplifiers in pixel arrays were performed before and after gamma radiation of up to 60 Mrad. Of special interest is the variation of the noise as a function of the sensor capacitance. We optimized the configuration of the amplifier for a fast rise time to adapt to the LHC bunch crossing period of 25 ns, and measured the timing characteristics including jitter. Our results indicate an adequate amplifier performance for monolithic structures used in HV-CMOS technology. The results have been incorporated in the next submission of a large-structure chip.

34 *Keywords:* HVC MOS, Silicon Strips, ATLAS phase-II upgrade

35 1. Introduction to ATLAS phase-II upgrade

36 The next major upgrade phase of the Large Hadron Collider (LHC) is cur-
 37 rently foreseen to be completed in 2024 [1]. It is called the High Luminosity-
 38 LHC (HL-LHC), and it aims to increase the integrated luminosity to about
 39 ten times the original LHC design luminosity, resulting in an additional inte-
 40 grated luminosity of around $2500\ \text{fb}^{-1}$ over ten years. These data will improve
 41 the precision of the measurement of the Higgs properties and enhance the
 42 sensitivity to search for new physics.

43 Silicon micro-strip sensors in the upgraded ATLAS experiment at the
 44 HL-LHC will be exposed to particle fluences of up to $2 \times 10^{15}\ n_{\text{eq}}/\text{cm}^2$ [2].
 45 Another challenge in HL-LHC operation is that the number of pile-up in-
 46 teractions per crossing will increase to 140, which is about ten times larger
 47 than for the current LHC. The existing ATLAS inner detector (ID) cannot
 48 maintain the tracking performance due to this huge increase in the channel
 49 occupancy. Therefore, a completely new ATLAS inner tracker is needed for
 50 the HL-LHC data taking. The sensors need to be designed with finer gran-
 51 ularity than the existing tracker to meet the challenges of very high pile-up

52 and to be able to reconstruct tracks in the core of multi-TeV jets.

53 **2. Introduction to CMOS based silicon sensor**

54 CMOS sensors can combine both silicon sensors and readout process-
55 ing circuitry on one single CMOS-chip, which will significantly simplify the
56 process of detector module building. CMOS sensors can provide high granu-
57 larity, and the pitch of the strip sensor can be reduced to below $50\ \mu m$. Due
58 to small feature size, this technology has the potential to be radiation hard.
59 The cost of CMOS sensor fabrication has the potential to be significantly less
60 compared to conventional planar sensors. Furthermore, CMOS-based sensors
61 collect charge from a thin depleted region so the sensor can be thinned down
62 to $50\ \mu m$ to reduce material. The major drawback of the CMOS-based sen-
63 sor is that it has a ten times lower total collected charge from a MIP than
64 the conventional planar sensor. It is crucial to integrate a low noise built-in
65 amplifier on the sensor chip to improve the signal to noise ratio of the system.

66 **3. Designing strip sensor with CMOS active pixel array**

67 In ATLAS Run1, the strip detector consists of double sided modules,
68 where a pair of conventional planar sensors are back-to-back with 40 mrad
69 stereo angle for the second coordinate measurement.

70 In order to use CMOS technology to build a strip sensor for the AT-
71 LAS upgrade, the basic design will be very different compared to the Run
72 1 detector. A full-size CMOS sensor is being designed for the ATLAS strip
73 upgrade as shown in Fig. 1 (a). It is a single-sided sensor, which consists
74 of 512 strips. Each strip has 32 segments that can provide the second co-
75 ordinate measurement. Each segment is an active pixel with analog frontend
76 (including built-in amplifier) and comparators.

77 The digital encoding is performed at the periphery of the CMOS chip.
78 There is a hit encoding structure manages hits on each strip. Its purpose is
79 to perform a sequential scan across the 32 segments of a strip and record the
80 segment that was hit. Strip encoding can select up to 8 hits per 128 strips
81 at 320 MHz per 25 ns bunch crossing. Preliminary physics simulation study
82 shows that this readout architecture can meet the occupancy specifications
83 for a strip detector for ATLAS Phase II physics.

Figure 1: (a) The preliminary design of pixel array for full-size strip sensor (b) The preliminary design of CMOS strip sensor chip with pixel arrays and periphery.

Figure 2: (a) A photo of HV-CHESS1 test chip (b) The layout of HV-CHESS1 test chip.

4. CMOS test chips

Two test chips have been fabricated in a AMS 0.35 μm high-voltage CMOS (HV-CMOS) process. The test chip HVStrip1 contains NMOS and PMOS transistors, a passive diode, and a 22x2 array of diode pixel sensors with active components implemented on the sensors. It can be used for a variety of active pixel characterizations.

Another test chip HV-CHESS1 contains several pixel matrices with different geometry, as well as built-in amplifier and stand-alone amplifier arrays. It permits pixel geometry optimization and characterization of a standalone built-in amplifier. A photo of HV-CHESS1 is shown in Fig. 2 (a), and the layout of HV-CHESS1 is shown in Fig. 2 (b).

5. Transistor performance in HV-CMOS chips

During the HL-LHC lifetime, the ATLAS strip detectors are expected to receive a dose of no more than 600 kGy of ionizing radiation. To understand

Figure 3: (a) The source-drain current in NMOS transistors of HVStrip1 chip as a function of gate voltage after gamma irradiation for (a) a linear layout transistor, (b) a circular layout transistor. The layout of a linear layout transistor and a circular layout transistor are also shown, and the gate in the yellow layer of the layout figure.

the radiation hardness of the electronics on CMOS chips, two type of NMOS transistor on HVStrip1 chip, as shown in Fig. 3, have been designed. The first one is a conventional linear transistor, while the other is designed in a circular (or enclosed) configuration which is expected to be radiation hard.

To test the radiation hardness, HVstrip1 chips were exposed to X-rays with a most probable energy of 35 keV [3]. Fig. 3 shows that source-drain current in NMOS transistors of HVStrip1 chip as a function of gate voltage after different doses of X-rays gamma irradiation. The source-drain current of NMOS transistor with linear layout increased significantly after gamma irradiation. This behavior is consistent with competing effects of oxide charge generation and the activation of interface traps [4]. At the same time, the circular layout NMOS transistors are not sensitive to gamma irradiation up to 600 kGy, which meets the radiation hardness requirements of the ATLAS phase II strip detector. Measurements of other devices on the HVStrip1 chip have been reported in Ref. [6, 7].

6. Built-in amplifier performance in HV-CMOS chips

A low noise built-in amplifier is used in the active pixel arrays in the HV-CHESS1 chip. The original design of amplifier is from Ivan Peric [5]. There are many configurable biases, including the bias in source followers (InSF) and feedback current (iFB).

In order to characterize the performance of this built-in amplifier, we use an external pulser to inject a fast signal on the amplifier input through a

(a)

Figure 4: The amplifier output pulse shape with fast pulses from external pulser as input.

120 built-in calibration capacitor (50 fF). The amplifier output pulse shape for
 121 different input signals is shown in Fig. 4.

122 Based on the amplifier output pulse shape, the response curve of this
 123 standalone built-in amplifier is characterized and shown in Fig. 5 (a). Total
 124 collected charge from a MIP in a HV-CMOS sensor is more than 1500 e^- .
 125 According to the response curve, the gain of this built-in amplifier is about
 126 1000 mV/fC at 1500 e^- input charge before irradiation. The measured gain
 127 agrees reasonably well with the results from simulations. The gain increased
 128 to 1900 mV/fC at 1500 e^- input charge after 3 Mrad gamma irradiation.

129 The radiation hardness study in HVStrip1 chip shows that the noise also
 130 increased with gamma irradiation dose as shown in Fig. 5 (b).

131 Combining two results in Fig. 5, the signal-to-noise ratio for a MIP signal
 132 in HV-CMOS sensor would have been above 50 if one could neglect the
 133 influence of the in pixel n-well capacitance.

134 The configuration of the amplifier is optimized for a fast rise time to adapt
 135 to the LHC bunch crossing period of 25 ns. The timing performance of the
 136 standalone built-in amplifier on HV-CHESS1 chip is also characterized using
 137 an external pulser. The measured signal rise time is shown in Fig. 6 (d).
 138 According to Fig. 6, the timing jitter using different thresholds on amplifier
 139 output as a function of input charge is evaluated and shown in Fig. 6 (a).
 140 The time walk effect is evaluated by comparing the time stamp of the signal

Figure 5: (a) Response curve of a standalone built-in amplifier on HV-CHESS1 chip. Due to uncertainty on capacitance load (C_{load}), three response curve predicted by simulations with different C_{load} are also provided. (b) The noise level of a standalone built-in amplifier on HVStrip1 chip as a function of gamma irradiation dose.

141 crossing threshold for different amounts of input charge. The uncertainty
 142 due to time walk effect is stable within $\pm 5\text{ns}$ as shown in Fig. 6 (b). The
 143 uncertainty due to time walk and jitter is significantly less than the LHC
 144 bunch crossing time (25 ns). In order to evaluate the dead time of each
 145 pixel, pulse width using different threshold on amplifier output as a function
 146 of input charge is also evaluated and shown in Fig 6 (c). A typical dead time
 147 for $1500 e^-$ input charge is less than 400 ns. Since there are 32 pixels in one
 148 strip in a full-size CMOS sensor, the effective dead time for a strip is 12.5 ns.

149 7. Active pixel response to Sr^{90} electrons

150 The active pixel performance in HV-CHESS1 chip is evaluated by expo-
 151 sure to beta radiation from Sr^{90} . The energy spectrum from the beta decay
 152 of Sr^{90} is a continuum up to its end point energy of 2.2 MeV . A scintillator
 153 was placed below the chip to select high energy minimum ionizing electrons.
 154 A typical pulse shape of active pixel response to Sr^{90} electrons is shown in
 155 Fig 7. The noise in an active pixel output is slightly higher than an isolated
 156 built-in amplifier due to the influence of the in pixel n-well capacitance. The
 157 signal-to-noise ratio for MIP signal in active pixel is still sufficient. The
 158 performance of passive pixels after irradiation is described in Ref. [8, 9];

Figure 6: (a) The timing jitter using different threshold on amplifier output as a function of input charge (b) The time walk at various amount of input charge (c) Pulse width using different threshold on amplifier output as a function of input charge. (d) Signal rise time

(a)

Figure 7: (a) A typical pulse shape of active pixel response to Sr^{90} electrons. The pixel size is $45 \mu m \times 800 \mu m$.

159 8. Summary

160 The HV-CMOS sensor technology is being developed as an alternative
161 solution for ATLAS Phase II strip detector upgrade. To withstand the much
162 harsher radiation in HL-LHC, two prototypes of radiation hard CMOS test
163 chips (HVStrip1 and HVCHES1) have been fabricated using the AMS H35
164 process .

165 The circular layout transistors are tested, and the results verify their
166 radiation hardness, fulfilling the requirements of HL-LHC operations.

167 The standalone built-in amplifier in the CMOS test chips has been char-
168 acterized. The uncertainty due to timing jitter and time walk effect is about
169 5 ns level, which is within a single LHC bunch crossing resolution (25 ns).
170 The gain of the built-in amplifier is verified to be sufficient to readout small
171 signal ($1500 e^-$), which is the lower limit of MIP signal from active pixel.

172 A prototype of a full-size strip sensor with fully digital readout is being
173 developed. It will be fabricated in the next few months, and the readout
174 architecture will be tested next year.

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