A Low-latency, Low-overhead Encoder for Data Transmission in the ATLAS Liquid Argon Calorimeter Trigger Upgrade

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Abstract

In this paper, we present the design and test results of an encoder integrated circuit for the ATLAS Liquid Argon Calorimeter trigger upgrade. The encoder implements a low-latency and low-overhead line code called LOCic. The encoder operates at 320 MHz with a latency of no greater than 21 ns. The overhead of the encoder is 14.3%. The encoder is an important block of the transmitter ASIC LOCx2, which is prototyped with a commercial 0.25- μm Silicon-on-Sapphire CMOS technology and packaged in a 100-pin QFN package.

Keywords: Front-end electronics for detector readout, Digital electronic circuits, Trigger concepts and systems (hardware and software)

1. Introduction

Optical data links have been successfully providing reliable and efficient data transmission in Large Hadron Collider (LHC) experiments in the past decade [1, 2]. The LHC is going to upgrade its luminosity to $5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$ in 2023. The upgrade requires the data links to provide much higher data rates with a reasonable power consumption and capability to operate in LHC's radiation environment. This brings a lot of challenges for designing the optical data link. The ATLAS Liquid Argon Calorimeter (LAr) will update its readout system to fully exploit the physics potential of the high luminosity in two phases. In the phase-I upgrade [3], its trigger system will be improved to select more efficiently signal events from background events by employing more sophisticated trigger algorithms. This requires the trigger system to transmit all digitized data to back-end with a reasonable latency. The LAr trigger upgrade requires installing 124 LAr Trigger Digitizer Boards (LTDBs). Each LTDB has 320 detector channels and transmits all the digitized data out of the front end through optical data links. The data rate for each LTDB is up to 204.8 Gbps [4]. A high-speed,

low-power and low-latency optical link is needed for the ATLAS LAr trigger system upgrade. This optical link is schematically shown in Fig. 1 [5]. The optical link on the transmitter side consists of a transmitter ASIC LOCx2 and a custom optical transmitter module MTx [6, 7]. The LOCx2 includes an encoder and a high-speed serializer. It receives data from the upstream ADCs and encodes the data for optical transmission. The encoder implements a custom line code LOCic [8]. The encoder scrambles the serial data to be DC balanced for optical transmission and also provides error detection code to check data integrity. The optical transmitter module converts the electrical signal to an optical signal transmitted through an optical fiber between the detector and the counting room. The optical signal is received and recovered to an electrical signal by an optical receiver in the counting room. The deserializer, usually embedded in an FPGA, recovers the parallel data from the serial data. The corresponding line code decoder recovers the original user data and checks if any error has happened during the data transmission.

The transmitter ASIC, LOCx2, is fabricated in a commercial 0.25 μm Silicon-on-Sapphire (SOS) CMOS technology for radiation-tolerance [9]. The layout of the LOCx2 chip is shown in Fig. 2 (a). Fig. 2 (b) shows the bonding photo of the chip package.

Fig. 3 is the block diagram of the LOCx2. As can be

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Figure 1: The block diagram of an optical data link.

Figure 2: The LOCx2 chip (a) and its bonding diagram on package (b).

seen in the figure, the encoder, named LOCic in diagram, serves as an interface between a custom 4-channel ADC [10] and the serializer. LOCx2 has two independent channels. Each channel receives data from the upstream ADCs, encodes the data, serializes the data, and provides a serial output at a speed of 5.12 Gbps. LOCx2 has the following functional blocks: two LOCic encoders, two 16:1 serializers, two Current Mode Logic (CML) drivers, a Phase-Locked Loop (PLL), and an Inter-Integrated Circuit (I²C) slave module. Each serializer takes the data from two ADC chips, for a total of 8 ADC channels. LOCx2 takes two signals from a GBTX chip [11], a 40 MHz LHC clock and a Bunch Crossing Identification (BCID) reset signal.

Figure 3: The block diagram of the LOCx2.

Besides the radiation tolerance requirement [12], a reduction of the overhead and latency are also very critical.

in this optical data link design. Low overhead allows the data transmission to be more efficient. The latency budget of the optical link is stringent due to the requirements of other sub-detector systems. In general, a shorter latency is preferred since the size of the event buffer used to store the data can be smaller. The latency budget of the optical link designed for the ATLAS LAr calorimeter trigger upgrade is 150 ns, not including the propagation time through the optical fiber (350 ns). The encoder and the decoder, usually contributing a significant amount to the latency of the optical link, have to be carefully designed. The requirements of the optical data link are shown in Table 1. For the whole link system of the ATLAS LAr, the BER of 10^{-12} corresponds to a dead time of 0.06%.

Table 1: The requirements of the optical data link

Power consumption (transmitter)	Radiation tolerance	BER	Latency
0.5 W/optical link	See [12]	$\leq 10^{-12}$	150 ns

In order to meet the requirements of the optical data link, the encoder design adopts the following approaches: First, to minimize the latency, the encoder keeps the data structure of the ADCs while adding in each frame a frame header and a frame trailer. Such a design eliminates extra data buffers and reduces the latency and hardware complexity. Moreover, the encoder is optimized to operate as fast as possible in order to reduce the latency. Since the $0.25 \mu\text{m}$ SoS CMOS technology digital library provided by foundry only guarantees 100 MHz operational speed, far below the desired 320 MHz, the encoder is manually laid out, not designed in digital design flow. Second, the encoder efficiently embeds 12-bit BCID information in the frame header, reducing the encoding overhead. Third, the control logic of the encoder is periodically reset to eliminate the potential accumulation of Single-Event Upsets (SEUs) for radiation tolerance. Moreover, the encoder is implemented using only static CMOS D Flip-flops and all internal configuration registers, part of the I²C slave shown in Fig. 3, are protected by triple modular redundancy. Due to the characteristics of the Silicon-on-Sapphire process, the CMOS circuits in this process have much lower cross section of SEE than the bulk CMOS. Even without redundancy design, the CMOS circuits have been proven to satisfy the requirements of ATLAS LAr Calorimeter front-end electronic system [15]. Fourth, the

Figure 4: Definition of the data frame.

input interface of the encoder is customized to adapt to the specific signal timing of the ADCs.

The remainder of the paper is organized as follows: Section 2 describes the proposed line code. The design of the encoder is described in Section 3. Section 4 discusses the encoder test setup and measurement results. Section 5 summarizes the paper.

2. The LOCic line code definition

A custom line code prepares the data of the ADCs for the serializer. The input data of the encoder come from two ADC ASICs [10]. Each ADC ASIC has four analog channels. Each analog channel samples four analog signals at 40 MS/s and digitizes them with a resolution of 12 bits. The output data of each analog channel in every conversion include 12-bit digitized data, 2-bit calibration data, and 2-bit dummy data (16 bits in total). The output data of each analog channel are then serialized and sent out at a data rate of 640 Mbps. The dummy bits will be replaced by the frame header and the frame trailer in the encoder, which will be discussed in the next section. Each ADC provides a clock of 320 MHz (SCK) to latch conveniently the serial data and a frame clock of 40 MHz (FCK) to indicate the boundary of each sample.

The LOCic frame is defined as the data which each serializer channel of LOCx2 transmits in a LHC clock cycle. Each LOCic data frame has 128 bits, including 8-bit frame header, 112-bit payload, and 8-bit frame trailer. The coding overhead is 14.3% (16/112). The frame header also efficiently transfers the BCID information for each frame. The first four bits of the frame header is a fixed code "1010" and the other four bits encodes 12-bit BCID information with two groups of 2-bit Pseudo-Random Binary Sequences (PRBSs). The first 2 bits are taken from the 2^5-1 PRBS and the other 2 bits from the 2^7-1 PRBS. Any consecutive 5 bits of the 2^5-1 PRBS determine the whole 2^5-1 PRBS and any consecutive 7 bits of the 2^7-1 PRBS determine the whole 2^7-1 PRBS. On the receiver side, if the four bits "1010" appear at the same position of four received consecutive frames and the following four bits in each of these four frames

meet the PRBS generation rule, we consider successful identification of frame boundary. The receiver recovers corresponding BCID information by combining the frame headers of four consecutive frames and looking up a table. The 8-bit frame trailer is an 8-bit Cyclic Redundant Checking (CRC) code calculated from the payload. The use of the CRC for error correction is described in section 3.2. The payload is scrambled before being transmitted, whereas the frame header and the frame trailer are not scrambled. The whole data frame in serial data stream is shown in Fig. 4. Channel 0 is firstly transmitted and Channel 7 is the last channel to be transmitted.

3. The Encoder design

Fig. 5 shows the block diagram of the encoder. The encoder is comprised of a First-In-First-Out (FIFO), a PRBS generator, a CRC generator, a scrambler, and a frame builder. The FIFO is custom designed to align the data coming from two ADCs. The FIFO has two Write clocks coming from two ADCs and one Read clock coming from the serializer. The FIFO can tolerate data skew of up to 3.125 ns between the two ADCs. The frame builder assembles the frame header, the frame trailer, and the scrambled data into a data frame.

Figure 5: The block diagram of the LOCic encoder.

Figure 6: The timing diagram of the input signals of the encoder.

3.1. The design of the FIFO

The timing diagram of the input signals of the encoder is shown in Fig. 6. Each encoder is connected to two ADCs (ADCs A and B). Each ADC outputs a frame clock (FCK) signal, a bit clock (SCK) signal of 320 MHz, and four data (Data0-Data3) signals of 640 Mbps. The High level of the FCK signal lasts for one half of the clock cycle of the SCK signal and the FCK signal repeats every LHC clock cycle of 25 ns or eight clock cycles of the SCK signal. The rising edge of the FCK signal indicates the start of a frame. As shown in Fig. 7, in FIFO the SCK signals are delayed by CMOS buffers, and then both edges of the delayed SCK are used to sample the FCK signal and all of the Data signals. Time skew of less than one clock cycle (i.e. 3.125 ns) of SCK may exist between the two ADCs connected to each encoder. Each encoder has a BCID generator that requires a common BCID reset signal. The High level of the BCID reset signal lasts for one LHC clock cycle (i.e. 25 ns) and the BCID reset signal repeats every 3564 LHC clock cycles. The BCID reset signal resets all BCID generators.

The block diagram of the FIFO is shown in Fig. 7. The FIFO is composed of two independent write controllers, a read operation controller, and two memories. Each memory has eight addressable memory units. Each unit is composed of four static D flip flops.

Figure 7: The block diagram of the FIFO.

The timing diagram of the FIFO is shown in Fig. 8. The Write Clock is a delayed signal of SCK. Each FCK signal triggers the write operation of the first bits of Data0-3

to the first memory unit (i.e. Address 0). Due to the skew between the two ADCs, one memory may be written earlier than the other. The read controller controls the read operations of both memories, hence the data from the two ADCs are aligned when they are read out. The read operation is triggered by the logical OR signal of two start signals, namely the earlier one. We adjust the time of the read operation to ensure that the read operation occurs when the data of the later ADC are written to the memory. Due to the limited memory depth, it is required that the later write operation is no more than one clock cycle later than the earlier one, which means that the skew between the two ADCs are no more than 3.125 ns. Both the write controller and the read controller are reset periodically by the FCK signals, eliminating the accumulation of potential SEUs in the controllers.

Figure 8: Timing diagram of the write and read operations.

3.2. The design of the CRC generator

The CRC code is calculated from the unscrambled payload to detect the radiation-induced SEUs. The SEU rate has been studied on the previous prototype of LOCx2 [15]. Two types of error are expected in the application. The first type is a single bit flip and the second one is a burst error of up to 80 bits following with a bit shift. It can be proved that with the scrambling algorithm to be discussed in Section 3.4, a single bit flip in the scrambled

Figure 9: The diagram of the CRC calculation.

data stream induces three bit flips in the descrambled data stream. Therefore, in order to detect a single-bit SEU, the error detection code must be capable of detecting up to three bit flips in the 112-bit payload. The CRC code $x^8 + x^5 + x^3 + x^2 + x + 1$ is chosen because it is the minimum-size (8 bits) CRC code which can detect up to three bit flips in a LOCic frame [13]. The CRC code can detect all single bit flips. The probability of a burst error or multiple-bit error generating the identical 8-bit CRC code is small, about 1/256. In other words, the CRC code can detect 99.6% of burst errors or multiple-bit errors.

The diagram of the CRC calculation is shown in Fig. 9. The symbol “+” in the diagram means the XOR operation. In each clock cycle of SCK (3.125 ns), the CRC generator calculates an 8-bit output based on the 16-bit input data and the 8-bit CRC calculated in the previous clock cycle (totally 24 input bits). Each output bit is an XOR operation of up to 17 input bits. The implementation of such a 17-input XOR gate corresponds to a chain of 5 stages of 2-input XOR gates. Simulation results indicate that it is difficult to ensure such a 17-input XOR operation at 320 MHz speed in the 0.25- μ m SoS CMOS technology. A pipeline technique is thus developed. With such a technique, it takes two clock cycles to calculate the 8-bit CRC results for each 16-bit input data. Compared to scrambling the payload, calculating the CRC code in the pipeline operation requires one more clock cycle. However, since the CRC code is attached to the scrambled data, the CRC code is used one clock cycle later than the scrambled data. Therefore, the pipeline technique actually causes no latency penalty.

3.3. The design of the PRBS generator

Since the frame clock is not transmitted through the optical fiber, there must be a mechanism for the receiver to identify the boundary of each ADC data frame. The frame header is used as both the frame boundary identifier and the BCID information carrier. The last four bits of the frame header is called the PRBS field, which encode 12-bit BCID information to align different channels. The PRBS field consists of two 2-bit PRBS data. The first 2-bit are taken from a repeating 2^5-1 PRBS, two bits per frame. Similarly, the second 2 bits are taken from a 2^7-1 PRBS. If combined with the previous data frame headers, the twisted 4-bit sequence repeats after 3937 ($=31 \times 127$) frames. This period is larger than 3564, the period of BCID. Each BCID has a corresponding unique sequence in the frame header if we combine a frame header with the previous frames. After BCID reaches its period, the PRBS field will be reset to its initial value of Frame 0.

In this way, the PRBS field is trimmed to the period of BCID. Because data frames are transferred to the back end without any trigger selection, the receiver can easily recovery 12-bit BCID information by combining consecutive frame headers.

Figure 10: A block diagram of the scrambler.

3.4. The design of the scrambler

The scrambler is used to create balanced codes without introducing extra bits and the far away backend receiver can use a descrambler to recover the data. The scrambling algorithm $x^{59} + x^{39} + 1$ [14] is used in the scrambler. The functional diagram of the scrambler with serial data input and output is shown in Fig. 10. However, both the input and output of the scrambler implementation are actually 16-bit parallel data. The parallel processing diagram is derived from Fig. 10 and is carefully verified in simulation. The basic logic operation of the scrambler is exclusive (XOR) operation (The symbol “+” in the diagram). In each clock cycle of SCK, the scrambler inputs 16 bits payload and produces 16 bits scrambled data.

4. Test of the encoder

The block diagram of the test setup is shown in Fig. 11. We use an Si5338 Clock Generator Evaluation Board (Part number Si5338-EVB) to generate two synchronized differential clock signals, at 40 MHz and 320 MHz, respectively. The 40 MHz clock is used as the reference input clock of the LOCx2 chip. The 320 MHz clock is used as the reference input clock of a Xilinx Kintex-7 FPGA KC705 Evaluation Board (Part number EK-K7-KC705-G). The output signals (5.12 Gbps serial data) of the test chip are sent to the FPGA for test.

The FPGA emulates four ADCs outputs and BCID reset as test chip input signals. The FPGA generates PRBS data, a SCK, and a FCK in the output format of the ADCs to emulate the ADC operation. The time among the data, SCK, and FCK of each ADC and the phase skew between two ADCs can be controlled by using programmable delay

cells through the Xilinx ChipScope Pro tool. The FPGA also generates a BCID reset, a common signal for all the encoders to align.

The FPGA also implements a link receiver that recovers the ADC data and checks if the recovered data have any errors. The link receiver consists of a Multiple-Gigabit Transceiver (MGT) (only the deserializer is used), a LOCic decoder, and an error logger. The deserializer converts the 5.12 Gbps serial data stream coming from each LOCx2 channel into 16-bit parallel data. Then the LOCic decoder recovers the original ADC data. The error logger records any errors occurring in the process. The error logger status is monitored by the Xilinx ChipScope Pro tool running on a computer connected to the FPGA board with a USB cable. A picture of test setup is shown in Fig. 12.

Figure 11: The block diagram of the test setup.

Figure 12: The test setup.

In the LOCic encoder test, the CRC field and BCID information were recovered completely in the decoder. Moreover, the payload generated in the ADC emulator was checked. For all chips under test, no error was observed during the test for ten minutes and the bit error rate was thus estimated to be less than 10^{-12} , the industrial standard, at a confidence level of 95%. One chip was tested error free for over a week.

The latency of the ASIC and the whole link has been measured. The latency of the whole link, including LOCx2 and the receiver implemented in an FPGA, not including optical transceiver and the optical fiber, is measured and summarized in Table 2. The latency of the whole link is from 68.2 to 74.3 ns. The contribution of the encoder is

from 17.8 to 21.0 ns. The latency variation comes from the FIFO and the deserializer because the phases of the internal clocks after each power cycle are uncertain. The total latency variation of 6.25 ns is much less than an LHC clock cycle of 25 ns. When the data are latched with a 40 MHz LHC clock and are sent to the trigger system, the latency will be a fixed value.

Table 2: The latency of the whole optical link

Function block			Latency (ns)
TX	LOCic Encoder	FIFO	8.4-11.6
		Scrambler & CRC gen	6.3
		Frame Builder	3.1
	Serializer		6.3
	Total LOCx2		24.1-27.3
RX	Deserializer		28.5-31.4
	LOCic Decoder	Data Extractor	9.4
		Descrambler	3.1
		CRC Check	3.1
	Total FPGA		44.1-47.0
Total optical link			68.2-74.3

5. Conclusion

An encoder ASIC implementing a custom line code of high speed serial data transmission is presented. The ASIC operates at 320 MHz with a latency of no greater than 21 ns, an overhead of 14.3% and a power consumption of about 96.3mW, meeting the design requirements. The encoder is integrated with a serializer and will be used in the ATLAS Liquid Argon calorimeter Phase I trigger upgrade.

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