The fabrication of carbon nanotube electronic circuits with dielectrophoresis

Zhigang Xiao^{*}, John Elike, Alishia Reynolds, Roderick Moten, and Xiang Zhao

Department of Electrical Engineering and Computer Science, Alabama A&M University,
Normal, AL 35762

Abstract

Single-walled carbon nanotubes (SWCNTs) are used widely in fabricating nanoelectronic devices because of their unique electrical properties. In this paper, we report the fabrication of carbon nanotube field-effect transistors (CNTFETs)-based inverter and ring oscillator electronic circuits using the dielectrophoresis (DEP) method. The electrical property of fabricated CNTFET-based devices was measured. The CNTFET-based inverter shown electrical transfer characteristics, while the CNTFET-based ring oscillator demonstrated oscillation characteristics, denoting that the CNTFET-based circuits can function well for the application of electronic circuits. The DEP-based fabrication method is scalable, and could be used for the wafer-scale fabrication of carbon nanotube electronic circuits.

Key words: Dielectrophoresis (DEP); single-walled carbon nanotubes (SWCNTs); carbon nanotube field-effect transistors (CNTFETs); inverter; ring oscillator.

^{*}Corresponding: Tel: 256-372-5679; Fax: 256-372-5855; Email: zhigang.xiao@aamu.edu.

I. Introduction

Single-walled carbon nanotubes (SWCNTs) have been investigated extensively in past years for the application of nanoelectronic devices [1-5], due to their unique electrical properties such as high current-carrying capacity, high mobility, and ballistic quantum transport [6, 7]. The carbon nanotubes (CNTs) with a diameter of several nanometers have a strong quantum-confinement effect in all directions perpendicular to the tube, resulting in ballistic transport in the tube for electrons and holes. These properties are not available in bulk electronic materials and can make CNT-based field-effect transistors (CNTFETs) operate much faster without energy dissipating in the tube [8].

Although there has been extensive research in the fabricating CNT-based devices such as single CNTFETs [9-15] and CNT electronic circuits [16-29], report on the wafer-scale fabrication of CNTFET-based electronic circuits is still highly interesting [30-33]. In this paper, we report the fabrication of carbon nanotube field-effect transistors (CNTFETs)-based inverter and ring oscillator electronic circuits using the dielectrophoresis (DEP) method. The inverter and ring oscillator circuits were implemented with only p-channel CNTFETs using the methodology of transistor-resistor logic [34], where a CNTFET was biased to function as a resistor. The CNTs were aligned onto the electrodes for the fabrication of CNTFET-based circuits using the electric field-directed dielectrophoresis (DEP). Dielectrophoresis (DEP) is a translational motion of neutral matter caused by polarization effects in a nonuniform electric field, and has been investigated theoretically and experimentally for deposition and alignment of CNTs recently [35-40]. Ultra-high density alignment of CNTs can be obtained with optimizing the ac frequency, the trapping time, and the CNT solution concentration in the DEP process [41, 42]. Impurities in

CNTs, especially the metal-containing impurity, could result in CNTFETs to be electrically shorted, and cannot be tolerated in the fabrication of electronic devices and circuits [43, 44]. The DEP-based alignment and deposition of CNTs has advantage over other methods, allowing ultra purification of CNTs with filtering the impurities in CNTs using various chemicals. In addition, the DEP-based fabrication of carbon nanotube electronic circuits is compatible with the integrated circuit (IC) fabrication, and could lead to the wafer-scale fabrication of CNT electronic devices and circuits.

II. Experimental Details

Ultra-purified SWCNTs (Carbon Nanotechnologies, Inc.) were used for the fabrication of CNTFET-based electronic circuits in this research. N-methyl pyrrolidone (NMP) was employed as the solvent for the purification and dispersion of SWCNTs, and ac dielectrophoresis (DEP) was used for the deposition and alignment of SWCNTs in the fabrication of CNTFET-based inverter and ring oscillator [45, 46]. The SWCNTs were subjected to a purification process before being applied to the device fabrication. 3 mg SWCNT powder was added to 20 ml NMP and sonicated for 1 h. After being sonicated in the NMP solution, the SWCNTs have a length ranging from about 0.5 to 4 μm . The SWCNT solution was then centrifuged at 14 000 rpm for 30 min. The resultant supernatant was decanted for the sedimented carbon nanotubes, which were again subjected to the purification cycle with fresh NMP. Figure 1 shows the SEM image of SWCNT mesh network after chemical purification and DEP-based deposition on silicon substrate. The prepared SWCNT–NMP solution was used in the following fabrication of devices.

Figure 2(a) shows the schematic of a CNTFET-based inverter electronic circuit, and Figure 3(a) shows the schematic of a three-stage CNTFET-based ring oscillator electronic circuit. Both circuits were implemented with p-channel CNTFETs only. Figure 4 shows the schematic cross section of the CNTFET. A set of five-pieces photo masks was designed for the fabrication of the CNTFET-based inverter and ring oscillator circuits. All the CNTFETs were designed to be identical and have the same channel length (3 μm) and width (10 μm). The photo masks were fabricated by Photoscience, Inc. As the substrates, we used three-inch-diameter n-type <100> silicon wafers (Virginia Semiconductor, Inc.). The silicon wafers were about 350- μm -thick with a resistivity of about 3 $\Omega\cdot\text{cm}$. The wafers initially were oxidized at 1100 $^{\circ}\text{C}$ for 20 minutes so to obtain a 200-nm-thick silicon dioxide layer using wet thermal-oxidation. Ultra-violet (UV) lithography and lift-off process were adopted for patterning in fabricating the devices. Shipley S1818 photo-resist was used in the UV lithography. All the thin films were deposited using electron-beam evaporation (background pressure of 2×10^{-7} Torr).

Two groups of Cr/Au electrodes including 5-nm-thick chromium (Cr) and 50-nm-thick gold (Au) were first fabricated for the deposition and alignment of SWCNTs. Dielectrophoresis was then applied to deposit and align SWCNTs across the gap of electrodes. A drop of the SWCNT–NMP solution was casted onto the electrodes, and an ac-bias with a peak-to-peak voltage of 10 V and frequency of 1 MHz was applied to the electrodes. The solvent was blown off the surface gently with nitrogen gas after 5 min. Figure 5(a) shows the SEM image of the two groups of Cr/Au electrodes with SWCNTs aligned across the gap of the electrodes, Fig. 5(b) shows an enlarged view of a pair of electrodes with SWCNTs. The two groups of electrodes were separated into individual pairs of electrodes without connecting to each other by etching away part of the Cr/Au

thin film, which connects the pairs of electrodes using the gold etchant and chromium etchant (Transene Company). A 20 nm-thick hafnium dioxide (HfO_2) thin film was deposited as the gate oxide via electron-beam evaporation. We used hafnium dioxide powder (99.9% purity; Alfa Aesar Company) as the source material for electron-beam evaporation. The HfO_2 film was grown at room temperature without substrate heating. The substrate holder was rotated at the speed of 20 RPM during the deposition. The process chamber had a pressure of 1×10^{-5} Torr during the deposition. The growth rate of the film was about $0.2 \text{ \AA/s}$, and an INFICON deposition monitor controlled the thickness of the film. A 500 nm-thick aluminum thin film was deposited using the e-beam evaporation, and etched to form the final metallization of the devices using the aluminum etchant (Transene Company). The CNTFET-based inverter also was fabricated together with the ring oscillator. After the fabrication was completed, we annealed the wafer at 350°C under a vacuum of 5×10^{-5} Torr for 20 minutes. The fabricated devices were imaged in a JEOL JSM-6610LV scanning electron microscope. We employed an Agilent precision source/measurement unit and Agilent mixed-signal oscilloscope to measure the electrical properties of the fabricated devices. The input of the first inverter was connected to the output of the third inverter for measuring the oscillation waveform. A voltage of 10 V was applied to the VDD in the inverter and ring oscillator for the electrical measurements, while a voltage of 0 V (grounded) was applied to the Bias. 10 V was selected as the power voltage (VDD) for the electrical measurements on the fabricated inverter and ring oscillator, which can make the inverter and ring oscillator to have a high enough power voltage for functioning well in the measurements.

III. Results and Discussion

Figure 2(c) is a SEM image of a fabricated CNTFET-based inverter, and Figure 2(d) is an enlarged view of the dielectrophoresis (DEP)-aligned single-walled carbon nanotube mesh networks connected between the gold electrodes in the inverter. The inverter consists of two identical CNTFETs. Figure 3(b) is a SEM image of a fabricated CNTFET-based ring oscillator. The ring oscillator consists of three CNTFET-based inverters (three stages).

Figure 6 shows the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for a fabricated CNTFET. The device presents electrical properties of a p-channel field-effect transistor (FET), which are similar to those of the p-type carbon nanotube transistors reported by other researchers [47, 48]. P-type transistors conduct holes when a negative voltage is applied to the gate. They do not conduct electron even at high positive gate voltages. The physical explanation for the IV characteristic in Fig. 6 is that the Fermi level at the metal (gold)-nanotube junction is closer to the valence band of the nanotube, leading to hole conduction and p-type behavior. The holes see a small barrier, thus they are able to tunnel through, where as the electrons see a much larger barrier, and are not able to tunnel [49]. The I_{DS} - V_{DS} curves in Fig. 6 show that the I_{DS} is very sensitive to the V_{GS} , and can be modulated by V_{GS} as shown in the Figure. With increasing V_{GS} negatively, I_{DS} values increase correspondingly. It is also shown that the I_{DS} value can be modulated up to about 175 μA at $V_{DS} = -8$ V and $V_{GS} = -12$ V. High I_{DS} values are important for making functional CNTFET-based electronic circuits. Although the I_{DS} value is lower compared to those reported by other researchers [50, 51], it is high enough for making the carbon nanotube inverter and ring oscillator to function well. The possible reason for the lower electrical current values is that the carbon nanotubes aligned by the DEP method with a high concentration SWCNT-NMP solution are not parallel to each other, and

form as networks, resulting in a lower electrical current value. Figure 7(a) shows a SEM image of carbon nanotubes aligned onto a pair of gold electrodes using the DEP method with a lower concentration solution (was diluted 30 times from the original solution and was further sonicated for 10 min), and Figure 7(b) shows the drain-source current (I_{DS}) as a function of the drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the fabricated CNTFET. The DEP method can make better alignment of carbon nanotubes across the electrodes with a solution of lower SWCNT concentration, but the lower concentration makes less carbon nanotubes aligned onto the electrodes, which achieve a lower electrical current. Figure 7(a) also shows that the SWCNTs are not single tube and have tube bundling (a single tube should have a diameter of several nanometers). High concentration solution was used for the device fabrication in this research. The solution with a higher SWCNT concentration makes carbon nanotube networks deposited between the electrodes with less alignment, but the dense carbon nanotube networks can achieve relatively higher electrical current values (compared Fig. 6 with Fig. 7). Figure 8 shows the I_{DS} - V_{GS} transfer curves of the CNTFET at various positive V_{DS} values and negative V_{DS} values. The transfer curves also show p-channel FET characteristics. The I_{DS} values decrease with decreasing V_{GS} values negatively, and was further depressed with increasing positive V_{GS} values. The physical explanation for the I_{DS} - V_{GS} transfer characteristic is that negatively increasing V_{GS} values make the Fermi level at the metal (gold)-nanotube junction closer to the valence band of the nanotube, and make the holes to see a smaller barrier, resulting in a higher I_{DS} value [49]. The ratio of I_{DS} at $V_{GS} = -12$ V and $+8$ V is about 100 for both cases of positive and negative V_{DS} .

Figure 9 shows the transfer characteristics of a functional CNTFET-based inverters at $V_{DD} = 10$ V and Bias = 0 V. The inverters present electrical transfer characteristics, showing that the output voltage can be switched from high to low with increasing the input voltage. The output voltage was switched from a high voltage of about 7 V to a low voltage of about 5.3 V, while the input voltage increased from -8 V to $+4$ V. The transfer characteristics is comparable with those obtained using the methodology of complementary metal-oxide semiconductor (CMOS) [22], where the output voltage was switched from a high voltage of 5 V to a low voltage of about 0.5 V, while the input voltage increased from -4 V to 0 V, and the transition of the output voltage from high to low happened around an input voltage of about -2 V. The transition of the output voltage from high to low in Fig. 9 happened around an input voltage of about -3.5 V, which is similar to the result in Ref. 22 (around -2 V). Figure 10 illustrates the oscillation waveform measured from a functional three-stage CNTFET-based ring oscillator at $V_{DD} = 10$ V. The oscillation has a frequency of about 2.5 kHz and a peak-to-peak magnitude of about 1.5 V.

IV. Summary

We successfully fabricated CNTFET-based electronic circuits using the ac dielectrophoresis (DEP) method. The CNTFETs, CNTFET-based inverters, and CNTFET-based ring oscillators demonstrated satisfactory electrical properties, indicating that the chemical purification and DEP-based alignment and deposition of SWCNTs can make SWCNT mesh networks for the fabrication of CNTFET-based electronic circuits. Although only SWCNT inverter and three-stage ring oscillator are demonstrated in this paper, other CNT electronic logic gates such as AND and OR logic gates can also be realized using the same design methodology and fabrication processes. The DEP-based patterning of SWCNTs in the device fabrication is simple

and scalable, and just needs one photo mask for the fabrication of electrodes, followed by the DEP process. The SWCNTs could be highly purified with the chemical-based purification method before the alignment and deposition of SWCNTs onto the electrodes. The DEP-based fabrication is also compatible with the conventional integrated circuit fabrication, and could be used for the wafer-scale fabrication of functional CNT electronic circuits.

Acknowledgements

Research carried out in part at the Center for Functional Nanomaterials, Brookhaven National Laboratory, which is supported by the U.S. Department of Energy, Office of Basic Energy Sciences, under Contract No. DE-SC00112704; the research is supported by National Science Foundation under Grant No. ECCS-1229312 and EPS-0814103.

References

- [1] Q. Cao and J. A. Rogers. Random networks and aligned arrays of single-walled carbon nanotubes for electronic device applications. *Nano Res.* Vol. 1, 259 (**2008**).
- [2] Q. Cao and J. A. Rogers. Ultrathin films of single-walled carbon nanotubes for electronics and sensors: A review of fundamental and applied aspects. *Adv. Mater.* Vol. 21, 29 (**2009**).
- [3] T. Rueches, K. Kim, E. Joselevich, G. Y. Tseng, C. L. Cheung, and C. M. Lieber. Carbon nanotube-based nonvolatile random access memory for molecular computing. *Science* vol. 289, 94 (**2000**).

- [4] J. Kong, J. Cao, H. Dai, and R. Anderson. Chemical profiling of single nanotubes: Intramolecular $p-n-p$ junctions and on-tube single-electron transistors. Appl. Phys. Lett. vol. 80, 73 (2002).
- [5] S. J. Kang, C. Kocabas, T. Ozel, M. Shimi, N. Pimparkar, M. Alam, S. Rotkin, and J. A. Rodger. High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes. Nature vol. 2, 230 (2007).
- [6] B. Q. Wei, R. Vajtai, and P. M. Ajayan. Reliability and current carrying capacity of carbon nanotubes. Appl. Phys. Lett. vol. 79, 1172 (2001).
- [7] C. T. White and T. N. Todorov. Quantum electronics: Nanotubes go ballistic. Nature vol. 411, 649 (2001).
- [8] S. Datta, Electronic transport properties in mesoscopic systems, Cambridge University Press, Cambridge, 1995.
- [9] M. C. LeMieux, M. Roberts, S. Barman, Y. W. Jin, J. M. Kim, and Z. Bao. Self-sorted, aligned nanotube networks for thin-film transistors. Science vol. 321, 101 (2008).
- [10] A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai. Carbon nanotube field-effect transistors with integrated ohmic contacts and high- κ gate dielectrics. Nano. Lett. vol. 4, 447 (2004).
- [11] R. V. Seidel, A. P. Graham, J. Kretz, B. Rajasekharan, G. S. Duesberg, M. Liebau, E. Unger, F. Kreupl, and W. Hoenlein. Sub-20 nm short channel carbon nanotube transistors. Nano. Lett. vol. 5, 147 (2005).
- [12] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke, and P. Avouris. Fabrication and electrical characterization of top gate single-wall carbon nanotube field-effect transistors. J. Vac. Sci. Technol. B vol. 20, 2798 (2002).

- [13] H. Wang, B. Cobb, A. Breemen, G. Gelinck, and Z. Bao, Highly stable carbon nanotube top-gate transistors with tunable threshold voltage, *Adv. Mater.* vol 26, 4588 (2014).
- [14] C. Qiu, Z. Zhang, D. Zhong, J. Si, Y. Yang, and L. Peng, Carbon nanotube feedback-gate field-effect transistor: suppressing current leakage and increasing on/off ratio, *ACS Nano* vol. 9, 969 (2015).
- [15] H. Wanga, P. Weib, Y. Lic, J. Hanb, H. Leec, B. Naabd, N. Liub, C. Wange, E. Adijantob, B. Teec, S. Morishitab, Q. Lib, Y. Gaoe, Y. Cuia, and Z. Baob, Tuning the threshold voltage of carbon nanotube transistors by n-type molecular doping for robust and flexible complementary circuits, *PNAS* vol. 111, 4776 (2014).
- [16] D. Sun, M. Timmermans, Y. Tian, A. Nasibulin, E. Kauppinen, S. Kishimoto, T. Mizutani, and Y. Ohno, Flexible high-performance carbon nanotube integrated circuits, *Nature Nanotechnology* vol. 6, 156 (2011).
- [17] L. Ding, Z. Zhang, S. Liang, T. Pei, S. Wang, Y. Li, W. Zhou, J. Liu, and L. Peng, CMOS-based carbon nanotube pass-transistor logic integrated circuits, *Nature Communications* vol. 3, 1 (2012).
- [18] B. Kim, S. Jang, M. Geier, P. Prabhumirashi, M. Hersam, and A. Dodabalapur, High-speed, inkjet-printed carbon nanotube/zinc tin oxide hybrid complementary ring oscillators, *Nano Lett.* vol. 14, 3683 (2014).
- [19] J. Zaumseil, Single-walled carbon nanotube networks for flexible and printed electronics, *Semicond. Sci. Technol.* vol. 30, 1(2015).
- [20] H. Chen, Y. Cao, J. Zhang, and C. Zhou, Large-scale complementary macroelectronics using hybrid integration of carbon nanotubes and IGZO thin-film transistors, *Nature Communication* vol. 5, 4097 (2014).

- [21] S. Park, M. Vosguerichian, and Z. Bao, A review of fabrication and applications of carbon nanotube film-based flexible electronics, *Nanoscale* vol. 5, 1727 (**2013**).
- [22] Z. Zhang, X. Liang, S. Wang, K. Yao, Y. Hu, Y. Zhu, Q. Chen, W. Zhou, Y. Li, Y. Yao, J. Zhang, and L. Peng, Doping-free fabrication of carbon nanotube based ballistic CMOS devices and circuits, *Nano Lett.* vol. 7, 3603 (**2007**).
- [23] M. Geier, P. Prabhumirashi, J. McMorro, W. Xu, J. T. Seo, K. Everaerts, C. Kim, T. Marks, and M. Hersam, Subnanowatt carbon nanotube complementary logic enabled by threshold voltage control, *Nano Lett.* vol. 13, 4810 (**2013**).
- [24] S. Lim, J. Jang, D. Bae, G. Han, S. Lee, I. Yeo, and Y. Lee, Contact resistance between metal and carbon nanotube interconnects: effect of work function and wettability, *Appl. Phys. Lett.* vol 95, 264103 (**2009**).
- [25] S. Heinze, J. Tersoff,* R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, Carbon nanotubes as schottky barrier transistors, *Phys. Rev. Lett.* vol. 89, 106801-1 (**2002**).
- [26] S. J. Tans, A. Verschueren, and C. Dekker. Room-Temperature Transistor Based on a Single Carbon Nanotube. *Nature* vol. 393, 49 (**1998**).
- [27] R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris. Single- and multi-wall carbon nanotube field-effect transistors. *Appl. Phys. Lett.* vol. 73, 2447 (**1998**).
- [28] Z. Chen, J. Appenzeller, Y. Lin, J. Sippel-Oakley, A. Rinzler, J. Tang, S. Wind, P. Solomon, P. Avouris, An integrated logic circuit assembled on a single carbon nanotube, *Science* vol. 311, 1735 (**2006**).
- [29] Y. Nosh, Y. Ohno, S. Kishimoto, and T. Mizutani, n-type carbon nanotube field-effect transistors fabricated by using Ca contact electrodes, *Appl. Phys. Lett.* vol. 86, 073105 (2005).

- [30] M. Shulaker, J. Rethy, T. Wu, L. Liyanage, H. Wei, Z. Li, E. Pop, G. Gielen, H. Wong, and S. Mitra, Carbon nanotube circuit integration up to sub-20 nm channel lengths, *ACS Nano* vol. 8, 3434 (2014).
- [31] M. Shulaker, G. Hills, N. Patil, H. Wei, H. Chen, H. Wong, and S. Mitra, Carbon nanotube computer, *Nature* vol. 501, 526 (2013).
- [32] D. Jariwala, V. Sangwan, L. Lauhon, T. Marks, and M. Hersam, Carbon nanomaterials for electronics, optoelectronics, photovoltaics, and sensing, *Chem. Soc. Rev.* vol. 42, 2824 (2013).
- [33] L. Peng, Z. Zhang, and S. Wang, Carbon nanotube electronics: recent advances, *Mater. Today* vol. 17, 433 (2014).
- [34] A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker. Logic circuits with carbon nanotube transistors, *Science* vol. 294, 1317 (2001).
- [35] L. Benedict, S. Louie, and M. Cohen, Static polarizabilities of single-wall carbon nanotubes, *Phys. Rev. B* vol. 52, 8541 (1995).
- [36] Z. Zhang, X. Liu, E. Campbell, and S. Zhang, Alternating current dielectrophoresis of carbon nanotubes, *J. Appl. Phys.* Vol. 98, 056103 (2005).
- [37] P. Li and W. Xue, Selective deposition and alignment of single-walled carbon nanotubes assisted by dielectrophoresis: from thin films to individual nanotubes, *Nanoscale Res. Lett.* vol 5, 1072 (2010).
- [38] B. Yang, Z. Yang, Z. Zhao, Y. Hu, J. Li, The assembly of carbon nanotubes by dielectrophoresis: Insights into the dielectrophoretic nanotube–nanotube interactions, *Physica E* vol. 56, 117 (2014).

- [39] A Naieni and A Nojeh, Effect of solution conductivity and electrode shape on the deposition of carbon nanotubes from solution using dielectrophoresis, *Nanotechnology* vol. 23, 495606 (2012).
- [40] A. Naieni and A. Nojeh, Dielectrophoretic deposition of carbon nanotubes: The role of field frequency and its dependence on solution conductivity, *Microelectronic Engineering* vol. 114 (2014).
- [41] S. Shekhar, P. Stokes, and S. Khondaker, Ultrahigh density alignment of carbon nanotube arrays by dielectrophoresis, *ACS Nano* vol. 5, 1739 (2011).
- [42] B. Sarker, S. Shekhar, and S. Khondaker, Semiconducting enriched carbon nanotube aligned arrays of tunable density and their electrical transport properties, *ACS Nano* vol. 5, 6297 (2011).
- [43] J. Tittmann-Otto, S. Hermann, J. Kalbacova, M. Hartmann, M. Toader, R. Rodriguez, S. Schulz, D. Zahn, and T. Gessner, Effect of cleaning procedures on the electrical properties of carbon nanotube transistors—A statistical study, *J. Appl. Phys.* vol. 119, 124509 (2016).
- [44] B. Liu, J. Liu, H. Li, R. Bhola, E. Jackson, L. Scott, A. Page, S. Irle, K. Morokuma, and C. Zhou, Nearly Exclusive growth of small diameter semiconducting single-wall carbon nanotubes from organic chemistry synthetic end-cap molecules, *Nano Lett.* vol. 15, 586 (2015).
- [45] Z. Xiao and F. E. Camino. The Fabrication of carbon nanotube field-effect transistors with semiconductors as the source and drain contact materials. *Nanotechnology* vol. 20, 135205 (2009).
- [46] Z. Xiao, H. Sharma, M. Zhu, and T. Pearson, Dielectrophoresis-assisted deposition and alignment of single-walled carbon nanotubes for electronic-device fabrication, *J. Vac. Sci. Technol. A*, vol. 28, 750 (2010).
- [47] P. Avouris, Carbon nanotube electronics, *Chem. Phys.* vol. 281, 429 (2002).

- [48] P. Avouris, R. Martel, V. Derycke, and J. Appenzeller, Carbon nanotube transistors and logic circuits, *Phys. B* vol. 323, 6 (**2002**).
- [49] R. Martel, V. Derycke, J. Appenzeller, S. Wind, and Ph. Avouris, Carbon nanotube field-effect transistors and logic circuits, *Proc. Of conference on Design automation*, pp. 94-98, **2002**.
- [50] M. Schröter, M. Claus, P. Sakalas, M. Haferlach, and D. Wang, Carbon nanotube FET technology for radio-frequency electronics: state-of-the-art overview, *IEEE J. Electron. Dev. Soc.* Vol. 1, 9 (**2003**).
- [51] A. D. Franklin, S. O. Koswatta, D. B. Farmer, J. T. Smith, L. Gignac, C. M. Breslin, S. Han, G. S. Tulevski, H. Miyazoe, W. Haensch, and J. Tersoff, Carbon nanotube complementary wrap-gate transistors, *Nano. Lett.* vol. 13, 2490 (**2013**).

Figure Captions:

Fig. 1. SEM image of SWCNT mesh network after chemical purification and DEP-based deposition on silicon substrate.

Fig. 2. (a) Schematic of a CNTFET-based inverter, which consists of two CNTFETs: The top one functions as a p-channel FET and the bottom one functions as a resistor; (b) An equivalent circuit; (c) SEM image of a fabricated CNTFET-based inverter; (d) SEM image of SWCNT mesh network connected between the electrodes.

Fig. 3. (a) Schematic of a circuit consisting of three CNTFET-based inverters, where the output of the first inverter is connected to the input of the second one, and the output of the second one is connected to the input of the third one; (b) SEM image of a fabricated circuit consisting three CNTFET-based inverters, where the inverters are connected in a chain.

Fig. 4. Schematic cross section of a CNTFET.

Fig. 5. (a) SEM image of two groups of electrodes with SWCNTs aligned onto the electrodes; (b) SEM image of an enlarged view.

Fig. 6. Drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for a CNTFET.

Fig. 7. (a) SEM image of SWCNTs aligned onto a pair of gold electrodes; (b) drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) and gate voltage (V_{GS}) for the fabricated CNTFET.

Fig. 8. Transfer characteristics of the CNTFET at $V_{DS} = +8V, +6V, +4V, +2V, -2V, -4V, -6V,$ and $-8V$, where the inset is the logarithmic plot of the transfer characteristics for $V_{DS} = +8V, +6V, +4V,$ and $+2V$.

Fig. 9. Transfer characteristics of a functional CNTFET-based inverters at $V_{DD} = 10V$.

Fig. 10. The oscillation waveform of a functional three-stage CNTFET-based ring oscillator at $V_{DD} = 10V$.

Fig. 1

Fig. 2

(a)

(b)

Fig. 3

Fig. 4

Fig. 5

Fig. 6

(a)

(b)

Fig. 7

Fig. 8

Fig. 9

Fig. 10

Graphical abstract