Fabrication and MOS interface properties of ALD AlYO₃/GeO_x/Ge gate stacks with plasma post oxidation

M. Ke^{a,b}, X. Yu^{a,b}, R. Zhang^a, J. Kang^{a,b}, C. Chang^{a,b}, M. Takenaka^{a,b}, and S. Takagi^{a,b}

^aDepartment of Electrical Engineering and Information Systems, The University of Tokyo, 7-3-1 Hongo, Bunkyo-ku, Tokyo 113-8656, Japan

^bJST-CREST

E-mail address of corresponding author: kiramn@mosfet.t.u-tokyo.ac.jp

Tel number of corresponding author: +81-3-5841-6733

Fax number of corresponding author: +81-5841-8564

Abstract

The realization of Ge gate stacks with thin equivalent oxide thickness (EOT), low interface state density (D_{it}) and small hysteresis is a crucial issue for Ge CMOS. In this study, we propose a new AlYO₃/GeO_x/Ge MOS interface, formed by atomic layer deposition (ALD) AlYO₃/Ge MOS structures with plasma post oxidation (PPO). Reduction in D_{it} by PPO is found for AlYO₃/Ge system. A 1.5-nm-thick AlYO₃/GeO_x/Ge interface with 1.25-nm EOT can provide a lower amount of the slow trap density, particularly in the valence band side of Ge, than the control Al₂O₃/GeO_x/Ge interface and the Y₂O₃/GeO_x/Ge interface. Deposition of any high- k films on the AlYO₃/GeO_x/Ge structure leads to the increase in the slow trap density to the same level, suggesting the influence of any traps at the interface between the high- k films and AlYO₃.

1. Introduction

Owing to the difficulty in further scaling of Si metal-oxide-semiconductor field-effect transistors (MOSFETs) caused by the physical limits of the Si material [1], Ge with higher electron and hole mobility than Si has become more and more attracting as a next generation MOSFET channel material. Here, one of the most difficult challenges in Ge complementary metal-oxide-semiconductor (CMOS) devices is the formation of gate stacks satisfying a variety of requirements such as thin equivalent oxide thickness (EOT), low interface state density (D_{it}), high channel mobility, long term reliability and so on.

As a promising gate stack, we have reported $Al_2O_3/GeO_x/Ge$ and $HfO_2/Al_2O_3/GeO_x/Ge$ structures realized by post plasma oxidation (PPO), where the GeO_x/Ge interface control layers are formed by oxidizing the Ge interfaces through the Al_2O_3/Ge and $HfO_2/Al_2O_3/Ge$ structures, respectively, by using ECR (electron cyclotron resonance) oxygen plasma [2-6]. These gate stacks have been shown to have EOT of 1 nm or thinner and low D_{it} of $\sim 10^{11} \text{ eV}^{-1} \text{ cm}^{-2}$ and to realize Ge-MOSFETs with high electron and hole effective mobility in such a thin EOT region [2-6]. However, one of the remaining critical issues for these MOS gate stacks is the existence of a large amount of slow traps and the resulting poor BTI (bias-temperature instability) characteristics [3, 5, 6], attributable to any defects in gate insulators including Ge oxides, Al_2O_3 and/or HfO_2 . Thus, the reduction in the amount of slow traps responsible for BTI and the significant improvement in the reliability lifetime are quite important. It has been recently reported, on the other hand, that Y-doped GeO_x interface layers fabricated by sputtering can provide the MOS interface properties with small hysteresis and low D_{it} [9-11]. These results suggest that appropriate doping of Y atoms into Ge oxides and Al_2O_3 near Ge interfaces can reduce the slow trap density and improve the BTI reliability.

In this study, we fabricate Ge MOS capacitors having Y_2O_3 and $AlYO_3$ gate insulators, deposited by using atomic layer deposition (ALD) system, with and without PPO. We analyze the physical properties such as the deposition rate, the permittivity and chemical structures by X-ray photoelectron spectroscopy (XPS). We systematically examine the effects of ALD Y_2O_3 and

AlYO₃ layers under the PPO process on the MOS interface properties such as D_{it} and the slow trap density in comparison with the control Al₂O₃/GeO_x/Ge MOS interfaces. The influence of the high-*k* films deposited on the AlYO₃ interfacial layers on the slow trap density is also examined.

2. Experiments

(100) Ge wafers were cleaned by de-ionized water, acetone and HF. After the pre-cleaning, 1-nm-thick Y₂O₃, 1.5-nm-thick Al₂O₃, 1-nm-thick AlYO₃ or 1.5-nm-thick AlYO₃ layers were deposited on Ge substrates at 300 °C by ALD using Al(CH₂)₃ and (CpMe)₃Y at 135 °C as the precursors and water. As for the AlYO₃ deposition, Al(CH₂)₃ and (CpMe)₃Y were supplied alternatively cycle by cycle, which is defined here as one AlYO₃ deposition unit cycle. Subsequently, 10s PPO using ECR plasma of Ar (9 sccm) and O₂ (3 sccm) mixture gas with 650W microwave power was carried out at 300 °C and 6x10⁻²Pa. The Ge 3d, Al 2p and Y 3d XPS spectra were taken for the AlYO₃/Ge structure with and without PPO in order to analyze the interface structure. In some capacitors, the 2nd ALD of high-*k* films including Y₂O₃, Al₂O₃ and HfO₂ was carried out at 300 °C and 150Pa, in order to decrease the gate leakage current or to examine the influence of the 2nd high-*k* films on slow trap properties. Note that we broke the vacuum between 1st and 2nd ALD process. Post deposition annealing (PDA) for 30 min at 400 °C in N₂ ambient was performed, followed by Au gate electrode and Al back contact formation by thermal evaporation. Also, we fabricated Al₂O₃/GeO_x/Ge MOS capacitors as the control samples for comparison.

3. Results and discussions

The Y₂O₃ and AlYO₃ film thickness was measured as a function of the ALD cycle by ellipsometry. The deposition rate of Y₂O₃ is estimated to be 0.12 nm/cycle, which is close to the previously reported value, 0.15nm/cycle [12]. Also, the permittivity estimated from the accumulation capacitance is found to be around 13, which is close to the ideal permittivity value of 15 [12] and twice higher than that of Al₂O₃. On the other hand, the deposition rate of AlYO₃

are estimated as 0.18 nm/unit cycle, where one unit cycle includes one supply cycle of $\text{Al}(\text{CH}_2)_3$ and one supply cycle of $(\text{CpMe})_3\text{Y}$. The permittivity is estimated to be around 9. We have confirmed that Al and Y atoms are included in the deposited films by using XPS Al 2p and Y 3d spectra. In order to examine the formation of interfacial GeO_x layer after PPO, we have measured XPS spectra for the 1.5-nm-thick AlYO_3/Ge structures before and after PPO in 10s. Fig. 1 shows the Ge 3d XPS spectra before and after PPO. The Ge 3d spectra for $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ structure fabricated by PPO through thin $\text{Al}_2\text{O}_3/\text{Ge}$ structures, taken from the previous result [2], are also shown for comparison. After PPO for AlYO_3/Ge , a peak at a binding energy of ~ 32 eV appears, as similar to that in the $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ structure formed by PPO, attributable to Ge sub-oxides, GeO_x [2-5]. This peak position seems to be different from the peak observed in previously reported $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces, which has been attributed to intermixing of Y and GeO_2 [9]. In contrast, we cannot find this Ge sub-oxides peak at the take-off angle of 5° , suggesting the existence of the Ge oxides near the Ge MOS interface. As a result, these results suggest that Ge oxides are formed between AlYO_3 and Ge, as similar to the $\text{Al}_2\text{O}_3/\text{Ge}$ system with PPO and thus, that the $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ structure can be formed by the PPO process. On the other hand, the position of the Ge sub-oxides peak for the 1-nm-thick $\text{Y}_2\text{O}_3/\text{Ge}$ interface with PPO, which is also shown in Fig.1, has been found to be the same as in Y- GeO_2 in the previously reported $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces [9], suggesting the intermixing of Y and GeO_2 .

Figs. 2 (a) and (b) show the C-V curves of 10-nm-thick $\text{Y}_2\text{O}_3/\text{Ge}$ capacitors without and with PPO, respectively. The $\text{Y}_2\text{O}_3/\text{Ge}$ capacitor without PPO has poor C-V curves with large frequency dispersion. It is observed, however, that the C-V curves are significantly improved after PPO with low frequency dispersion and sharp change in the capacitance values. Fig. 3 shows the energy distributions of D_{it} of $\text{Y}_2\text{O}_3/\text{n-Ge}$ and $\text{Y}_2\text{O}_3/\text{p-Ge}$ MOS capacitors with and without PPO. Here, D_{it} was evaluated by the conductance method. The energy distribution of D_{it} of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{n-Ge}$ MOS capacitors is also shown for comparison. It is found that D_{it} is significantly reduced by PPO down to the same level as in $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ interface [2-5], indicating the effectiveness of PPO even for the $\text{Y}_2\text{O}_3/\text{Ge}$ system. However, a clear drawback of the $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS capacitors,

seen in Fig. 2(b), is the large hysteresis and the resulting large amount of slow traps, which might be any defects generated in $\text{Y}_2\text{O}_3/\text{GeO}_x$ interfacial layers. It has been reported, on the other hand, that Y-doped GeO_x/Ge MOS interfaces fabricated by sputtering of Y-doped GeO_2 with the optimum Y content has small hysteresis [9-11]. Thus, we can judge from these results that further refined control of intermixing of GeO_2 and Y and/or defect control of Y_2O_3 films are strongly needed to reduce slow trap density.

For this purpose, we introduce the AlYO_3/Ge interfaces instead of the $\text{Y}_2\text{O}_3/\text{Ge}$ ones. Figs. 2 (c) and (d) show the C-V curves of 1.5-nm-thick AlYO_3/Ge MOS interfaces with and without PPO. The CET values of the AlYO_3/Ge MOS interfaces with and without PPO are estimated to be 1.46 and 1.65 nm, respectively. It is observed that the AlYO_3/Ge MOS interfaces have much smaller frequency dispersion and smaller hysteresis than the $\text{Y}_2\text{O}_3/\text{Ge}$ MOS interfaces. Particularly, the C-V curves of the $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces after PPO are found to have much smaller hysteresis than those before PPO and $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ after PPO. Actually, this larger hysteresis of $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ is attributable not only to the thicker gate insulator, but also to the larger amount of slow trap density, which will be quantitatively discussed through the comparison between 9-nm-thick $\text{Y}_2\text{O}_3/1\text{-nm-thick } \text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ and 9-nm-thick $\text{Y}_2\text{O}_3/1\text{-nm-thick } \text{AlYO}_3/\text{GeO}_x/\text{Ge}$ gate stacks in Fig. 10. Fig. 4 shows the energy distributions of D_{it} of $\text{AlYO}_3/\text{n-Ge}$ MOS capacitors with and without PPO. It is also found that D_{it} is significantly reduced by PPO, as similar to the $\text{Y}_2\text{O}_3/\text{Ge}$ MOS interfaces. As a consequence, we can conclude that both interface traps and slow traps can be reduced in the $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces thanks to the GeO_x interfacial layers introduced by applying PPO to AlYO_3/Ge structures.

In order to quantitatively evaluate the density of slow traps, we experimentally measure the relationship between the effective slow trap areal density, ΔN_{fix} , and the effective electric field across gate insulators, E_{ox} , which has recently been proposed as an effective method to estimate the slow trap density responsible for BTI reliability [8]. Fig. 5 schematically shows how to evaluate ΔN_{fix} and E_{ox} on a basis of C-V characteristics of MOS capacitors. In conventional C-V measurements with forward and backward voltage scans, the amount of hysteresis, ΔV_{hys} , is

measured with changing $V_{\min}$ with holding constant $V_{\max}$, where $V_{\min}$ and $V_{\max}$ mean the minimum and the maximum gate voltages in the gate voltage scan of the C-V curve, allowing us to provide the effective amount of the slow trap density as a function of E_{ox} [8]. Here, E_{ox} and ΔN_{fix} are given by

$$E_{ox} = (V_{\min} - V_{FB})/CET,$$

$$q \Delta N_{fix} = C_{ox} \Delta V_{hys},$$

where V_{FB} , CET, q and C_{ox} is the flat band voltage, the accumulation capacitance equivalent thickness, the elementary charge and the accumulation capacitance, respectively. In the present measurement of p-Ge MOS capacitors, $V_{\max} - V_{FB}$ is taken to be 1 V. The decrease in $V_{\min}$ and the increase in E_{ox} lead to the increase in the hysteresis and the resulting increase in the density of responsible slow traps.

Fig. 6 shows ΔN_{fix} of the $AlYO_3$ /p-Ge interface with and without PPO as a function of E_{ox} . It is found that PPO can reduce the amount of slow traps in lower E_{ox} and can yield steeper slope in the ΔN_{fix} - E_{ox} relationship, which is favorable to the BTI reliability [8]. This result means that the PPO process and/or the formed interfacial GeO_x in the $AlYO_3/GeO_x/Ge$ MOS interfaces can contribute to the reduction in the slow trap density in a deeper energy range, while the slow trap density tends to increase with approaching the energy toward the valence band edge of the gate insulators. Fig. 7 shows the comparison in ΔN_{fix} of the $AlYO_3/GeO_x$ /p-Ge and $AlYO_3/GeO_x$ /n-Ge MOS interfaces. We also plot the data reported for Al_2O_3/GeO_x /n-Ge MOS interfaces [8] as a reference. The results confirm us that the p-Ge MOS capacitor has a smaller amount of slow traps than the n-Ge one, which has the same level of the slow trap density reported for Al_2O_3/GeO_x /n-Ge MOS interfaces. This finding indicates that almost one order of the magnitude higher density of slow traps exists near the conduction band of Ge than the valence band. In order to more directly compare the difference between the $AlYO_3/GeO_x/Ge$ and the $Al_2O_3/GeO_x/Ge$ MOS interfaces, the slow trap density is evaluated for the two types of the MOS capacitors fabricated at the same time. Fig. 8 shows ΔN_{fix} of the 1.5-nm-thick $AlYO_3/GeO_x/Ge$ and

1.5-nm-thick $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ interfaces for both n- and p-Ge substrates. It is found that ΔN_{fix} of the $\text{AlYO}_3/\text{GeO}_x/\text{p-Ge}$ interface is significantly lower than that of $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{p-Ge}$ interface, while the reduction in ΔN_{fix} for n-Ge is small for the $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ interface. These results mean that AlYO_3 -based gate stack can effectively improve the amount of slow traps in the valence band against the conventional $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ interfaces.

Next, in order to examine the influence of the 2nd high- k films deposited on the original $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ interface on the slow trap density, ΔN_{fix} is evaluated for the MOS capacitors with the 2nd ALD films having the different thickness and the different high- k materials. Fig. 9(a) shows ΔN_{fix} of the 1.5-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces with 1-nm-thick 2nd ALD Y_2O_3 , 1-nm-thick 2nd ALD Al_2O_3 and without any 2nd ALD high- k films. The capacitors with the 2nd ALD high- k films have higher ΔN_{fix} than the 1.5-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ without any additional films. We suppose that there can be three possible mechanisms for the increase in ΔN_{fix} after the 2nd ALD high- k film deposition. One is any degradation of the underlying oxide and/or interface induced by the 2nd high- k deposition. The second mechanism is the trap generation at the interface between the 1st and the 2nd high- k layers, attributable to any reaction during the 2nd high- k deposition and/or the vacuum break between the 1st and the 2nd ALD process. The third possible mechanism is trapping into the 2nd high- k films, irrespective of Al_2O_3 or Y_2O_3 .

In order to examine the possible physical origin for this increase in ΔN_{fix} after the 2nd ALD high- k film deposition, different 2nd high- k films have been deposited on 1-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces. Fig. 9(b) shows the relationship between E_{ox} and ΔN_{fix} of the 1-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces with 4-nm-thick 2nd ALD Y_2O_3 , Al_2O_3 and HfO_2 . We have also found that the 4-nm-thick 2nd ALD Y_2O_3 , Al_2O_3 and HfO_2 films provided almost the same level of the slow trap density for both n and p-Ge substrates, meaning that the traps existing in a region deeper than ~ 2 nm from the MOS interfaces can contribute to the hysteresis and BTI reliability. Furthermore, the 2nd Y_2O_3 film thickness dependence of ΔN_{fix} is evaluated for 2nd $\text{Y}_2\text{O}_3/\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces. Fig. 10 shows ΔN_{fix} for $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces with the 9-, 3- and 1-nm thick 2nd Y_2O_3 films. It is found that there is almost no dependence of

ΔN_{fix} on the thickness of the 2nd Y_2O_3 films. These results indicate that trapping into the 2nd high- k films is not a main reason for the increase in ΔN_{fix} . As a result, the two possible mechanisms of the MOS interface degradation and the trap generation between the original AlYO_3 films and the 2nd ALD high- k films can be regarded as responsible for the increase in ΔN_{fix} after the 2nd ALD high- k film deposition. However, further examinations would be still needed to specify the degradation mechanism.

In addition, the relationship between E_{ox} and ΔN_{fix} of the 9-nm-thick Y_2O_3 /1-nm-thick $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS interface is also plotted for comparison with that of the 9-nm-thick 2nd Y_2O_3 /1-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces in Fig. 10. It is clearly observed that ΔN_{fix} of the 10-nm-thick $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS interface is much higher under the similar gate capacitance than that of the MOS interface with the AlYO_3 interfacial layer. This result confirms us that the larger hysteresis and higher ΔN_{fix} of $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ is attributed to the larger amount of slow trap density, indicating the importance of the AlYO_3 interfacial layer.

The amount of ΔN_{fix} with the different PPO time for the AlYO_3/Ge MOS interfaces is also evaluated to examine the effects of the interfacial Ge oxides on the hysteresis. Fig.11 shows the PPO time dependence of ΔN_{fix} . The longer PPO time can lead to a slight decrease in the amount of slow traps, meaning that the thicker GeO_x layer can reduce the density of traps accessible from Ge surfaces. This finding is similar to the fact that thicker GeO_x layer can reduce D_{it} [3-5]. However, the thickness of the fabricated GeO_x interfacial layers and the chemical structure including the existence of Y atoms into GeO_x have not been characterized yet in this study. Thus, further investigation of the characterization of the gate stack structure and the identification of slow traps are strongly needed to optimize the structures and the formation process of the high- k / $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ gate stacks utilizing with PPO for thin EOT Ge-MOSFETs.

4. Conclusion

The characteristics of $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ and $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS gate stacks with PPO have been experimentally examined. The PPO process is found to effectively reduce D_{it} for

$\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ and $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS gate stacks. However, the hysteresis for $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ structure is reduced, while that for $\text{Y}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ significantly increases. We have demonstrated lower D_{it} and lower slow trap density for the 1.5-nm-thick $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces fabricated by PPO than those for the $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ interface and the $\text{Y}_2\text{O}_3/\text{Ge}$ MOS interface. The slow trap density responsible for the hysteresis for $\text{AlYO}_3/\text{GeO}_x/\text{p-Ge}$ MOS capacitors is one order of the magnitude lower than that for the n-Ge MOS capacitors, as similar to the $\text{Al}_2\text{O}_3/\text{GeO}_x/\text{Ge}$ MOS capacitors. The $\text{AlYO}_3/\text{GeO}_x/\text{Ge}$ MOS interfaces with 2nd high- k films is found to exhibit the higher slow trap density by almost the same level, independent of the 2nd high- k film material and thickness, suggesting the possibility of the relevance of the MOS interface degradation during the 2nd high- k deposition and/or any traps at the interface between the original $\text{AlYO}_3/$ and the 2nd high- k films.

Acknowledgements

This work was partly supported by a Grant-in-Aid for Scientific Research (No. 26249038) from the Ministry of Education, Culture, Sports, Science, and Technology in Japan and JST, CREST.

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Figure captions

Fig. 1: Ge 3d XPS spectra of 1.5-nm-thick AlYO₃/Ge interfaces with and without PPO, and a 1-nm-thick Y₂O₃/Ge interface with PPO. The Ge 3d XPS spectra of the Al₂O₃/GeO_x/Ge interfaces, previously reported [2], are also shown as a reference.

Fig. 2: C-V curves of 10-nm-thick Y₂O₃/Ge MOS capacitors (a) without and (b) with PPO and 1.5-nm-thick AlYO₃/Ge MOS capacitors (c) without and (d) with PPO. The measurement frequency was varied from 1 k, 10 k, 100 k to 1 MHz.

Fig. 3: Energy distributions of D_{it} in the 10-nm-thick Y₂O₃/n-Ge and Y₂O₃/p-Ge MOS capacitors with and without PPO.

Fig. 4: Energy distributions of D_{it} in the 1.5-nm-thick AlYO₃/p-Ge MOS capacitor with and without PPO.

Fig. 5: Schematic diagram of ΔN_{fix} evaluation on a basis of C-V measurements of a p-Ge MOS capacitor with changing the minimum gate voltage, V_{min} , and holding the maximum gate voltage, V_{max} . Here, ΔV_{hys} , ΔN_{fix} , E_{ox} , V_{FB} , CET, q and C_{ox} is the amount of hysteresis, the effective slow trap areal density, the effective electric field, the flat band voltage, the accumulation capacitance equivalent thickness, the elementary charge and the accumulation capacitance, respectively.

Fig. 6: Relationship between E_{ox} and ΔN_{fix} of 1.5-nm-thick AlYO₃/Ge MOS interface with and without PPO.

Fig. 7: Relationship between E_{ox} and ΔN_{fix} of 1.5-nm-thick AlYO₃/GeO_x/n-Ge and 1.5-nm-thick AlYO₃/GeO_x/p-Ge MOS interfaces. The ΔN_{fix} - E_{ox} relationships of an Al₂O₃/GeO_x/n-Ge MOS

capacitor and a Si capacitor reported by the other group [8], are also shown in comparison.

Fig. 8: Relationship between E_{ox} and ΔN_{fix} of 1.5-nm-thick $AlYO_3/GeO_x/p\text{-Ge}$ and $n\text{-Ge}$ MOS capacitors and 1.5-nm-thick $Al_2O_3/GeO_x/n\text{-Ge}$ and $p\text{-Ge}$ MOS capacitors.

Fig. 9: (a) Relationship between E_{ox} and ΔN_{fix} of the 1.5-nm-thick $AlYO_3/GeO_x/Ge$ MOS interfaces with 1-nm-thick 2nd ALD Y_2O_3 , 1-nm-thick 2nd ALD Al_2O_3 and without any 2nd ALD high- k films. (b) Relationship between E_{ox} and ΔN_{fix} of the 1-nm-thick $AlYO_3/GeO_x/Ge$ MOS interfaces with 4-nm-thick 2nd ALD Y_2O_3 , Al_2O_3 and HfO_2 .

Fig. 10: Relationship between E_{ox} and ΔN_{fix} of 1-nm-thick $AlYO_3/GeO_x/Ge$ MOS interfaces with 9-, 3- and 1-nm-thick 2nd Y_2O_3 films, and the 9-nm-thick $Y_2O_3/1\text{-nm-thick } Y_2O_3/GeO_x/Ge$ MOS interface.

Fig. 11: Relationship between E_{ox} and ΔN_{fix} of 9-nm-thick 2nd $Y_2O_3/1\text{-nm-thick } AlYO_3/GeO_x/Ge$ with different PPO time of 30s, 60s and 90s.

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Fig. 11