Fabrication and Characterisation of Suspended Narrow Silicon Nanowire Channels for Low-Power Nano-Electro-Mechanical (NEM) Switch Applications

L. Boodhoo^a, L. Crudgington^a, H. M. H. Chong^a, Y. Tsuchiya^a, Z. Moktadir^a, T. Hasegawa^b, H. Mizuta^{a,c}

^a Nano Research Group, Electronics and Computer Science, University of Southampton, Southampton, SO17 1BJ, UK

^b Atomic Electronics Group, National Institute for Materials Science, Japan

^c School of Materials Science, Japan Advanced Institute of Science and Technology, Japan

e-mail: lab406@ecs.soton.ac.uk

Keywords: NEMS, suspended, nanowire, narrow channel, double gate, double suspension, low power, CMOS compatible

Abstract

Suspended silicon nanowires with narrow (~10 nm) conduction channel are fabricated and characterised for further development of low power nano-electro-mechanical (NEM) switching devices using CMOS compatible fabrication. Double suspension fabrication process using an amorphous silicon sacrificial layer and xenon difluoride etching is employed for thermally-oxidised suspended Si nanowire channels. Device current-voltage characteristics demonstrate depletion mode operation of heavily doped nanowires with an on/off ratio of 10^5 and a threshold voltage of -1.8 V. In plane electromechanical pull-in to side gate is demonstrated and confirmed to be consistent with finite element analysis.

1. Introduction

Leakage current in complementary metal-oxide-semiconductor (CMOS) technology below the 45 nm feature scale is expected to lead to increased power dissipation. To maintain previous performance increase rates, metal-oxide-semiconductor field effect transistor (MOSFET) technology scaling is still continuing. Due to increased power dissipation, MOSFET fabrication is driving towards innovations in materials and new device structures for logic circuits [1].

Nano-electro-mechanical systems (NEMS) are considered as potential candidates for low power switch integration due to the possibility for steep subthreshold slopes [2] and near zero leakage currents [3]. Existing NEMS designs include graphene [4], [5], [6], carbon nanotubes [7], silicon carbide [8], silicon [9] and metal [10], [11]. Additionally, the possibility of exploiting the stored mechanical energy has been proposed for creating two stable state switches [12], [13]. Progress of contact NEMS switches and the relationship of the stiction force and the electromechanical forces are detailed in [14]. Other competing technology solutions include magnetic coupled spin-torque devices [15], [16], resistive random access memory (ReRAM) [17], phase change memory (PCM) [18], magnetic tunnel junction devices (MTJs) [19], [20]. However, these candidates potentially come with complex fabrication, exotic material requirements and CMOS fabrication compatibility issues.

The motivation of this work is the design and fabrication of non-volatile bistable low power sleep transistors for advanced power management in logic circuits. This paper describes fabrication and characterisation of suspended silicon nanowire devices previously reported in [21]. The aim is to create a bistable non-volatile NEMS switch which exploits stiction upon mechanical contact with either side gate electrode. Two potential switching mechanisms are considered for these devices: i) direct electrical contact from gate to drain; ii) depletion induced

in the nanowire by opposite doping profile at *one* gate electrode, requiring insulated surfaces during mechanical contact.

Electrostatic current modulation is observed in a suspended conducting channel with heavy doping and consequent linear current-voltage characteristics. The fabricated devices exhibit excellent electrical isolation from two opposing side gate electrodes. Measured electro-mechanical pull-in conforms to expected results verified by finite element method simulation. Device destruction is observed after lateral electromechanical pull-in due to the high pull-in voltage required for the prototype doubly clamped beam design. This result is compared with results of devices fabricated using lightly doped silicon which avoid the joule heating induced beam destruction observed in the heavily doped devices.

The suspended silicon nanowire device configuration presented here consists of an oxidised silicon channel with a 42 nm by 50 nm total cross section and length of 1800 nm. Source and drain electrodes are at either end of the suspended channel, which is flanked by two opposing side gates with a separating air gap of ~ 50 nm. This is illustrated in Fig. 1.

Fig. 1: Schematic diagram of suspended silicon nanowire configuration [21]. The suspended nanowire conducting channel is 1800 nm in length with a 42 by 50 nm cross section. Two opposing side gates, separated by a ~ 50 nm air gap, are used to electrostatically actuate on and off current conditions.

2. Fabrication

Suspended silicon nanowire devices are fabricated on ultrathin silicon-on-insulator (SOI) substrates with a device layer thickness of ~ 50 nm. The device layer is phosphorus doped to a concentration of $\sim 1 \times 10^{19} \text{ cm}^{-3}$ using spin-on phosphorosilica film (2500 RPM for 60 s) followed by annealing at 925°C for 8 minutes.

Nanoscale device features are patterned by electron beam lithography using a JEOL 9300 JBX Electron Beam Lithography System. Ebeam exposure of 29 nm hydrogen silsesquioxane (HSQ) realises channel widths of around 42 nm on 50 nm thickness SOI. Smallest features are patterned with a fixed dose of $1750 \mu\text{C}/\text{cm}^2$ at 1 nA beam current, 5 nm spot size and shot pitch of 4 nm. To reduce ebeam exposure times, large features are patterned during a second exposure using a 10 nA beam current, 24 nm spot size, 20 nm pitch and process error correction with on-chip global alignment marks.

An Oxford Instruments capacitive reactive ion etching (RIE) tool is used to etch device features using sulphur hexafluoride (SF_6) and oxygen (O_2) chemistry. Both gases are introduced to the chamber at a constant rate of 36 sccm, RF power is maintained at 100 W. This results in vertical sidewalls and an etch rate of around 1.5 nm/s.

The silicon nanowire channel is suspended using hydrofluoric (HF) acid under-etching of the 200 nm thick buried oxide (BOX) layer using an Idonus HF vapour phase etcher. HF etch is performed at 45°C. The resultant etch of the BOX layer is variable, 5 minute exposure cycles etch between 30 nm and 60 nm, ellipsometry and SEM imaging are used to monitor the etch progress between etch cycles. Vapour phase etching eliminates capillary force induced stiction to the substrate which is observed when under-etching using liquid etchant [22]. After the first suspension stage a thin oxide layer is thermally grown on the surface of both side gates and the suspended nanowire at 825°C for 12 minutes under an O_2 flow of 5 slm (Fig. 2(a)). This process is used to passivate the silicon nanowire and to create an insulating layer.

Fig. 2: Cross section illustrations of the critical stages of fabrication for the suspended oxidised silicon nanowires. (a) After suspending the nanowire by vapour HF and thermal oxide growth, (b)

slow deposition of the amorphous silicon sacrificial layer is critical in order to ensure the suspended nanowire is not damaged and that a high-density protective film is achieved. (c) Patterns of varying sizes are prepared before metallisation using AZ2070 photoresist to etch through the a-Si and the thermal oxide layer. (d) By design, aluminium contact pads overlap the thermal oxide layer to protect the underlying silicon device layer during the final a-Si etching step. (e) Final XeF₂ vapour release stage etches sacrificial a-Si but not the 50 nm silicon device layer because of the thin thermal oxide surface.

A ~600 nm thick sacrificial layer of amorphous silicon (a-Si) is then deposited by plasma enhanced chemical vapour deposition (PECVD) to protect the suspended silicon nanowire channel during metallisation (Fig. 2(b)). The sacrificial a-Si layer is fabricated using an Oxford Instruments PlasmaLab System 100. The system uses capacitively coupled RF plasma at 13.56 MHz to disassociate source gases silane (SiH₄) and hydrogen (H₂) for deposition onto a heated substrate (250°C). 50 sccm SiH₄ and 50 sccm H₂ flow rates, 350 mTorr chamber pressure and 10 W RF power produce a high-density film at a slow deposition rate of ~0.26 nm/s. The resultant film is optimised for xenon difluoride (XeF₂) etching whilst minimising surface stresses within the layer. High amorphous silicon deposition rate conditions will result in a low-density film with high levels of bond-length disorder. This has been found to become saturated with photoresist solution used during subsequent fabrication processes, causing regions of unetched amorphous silicon after xenon difluoride treatment. The residual a-Si structures have feature sizes in the 10s of nanometres up to several 100 nm; these are large in relative proportion to the 50 nm features of the suspended silicon nanowire devices.

Contact holes through to the device layer are patterned by photolithography using AZ2070 photoresist. First, holes are etched through the a-Si to the thermal oxide layer (Fig. 2(c)). The a-Si layer is etched using XeF₂ vapour, this step uses the thermal oxide layer to act as a stopping material for the gas phase etchant. The XeF₂ has near infinite etch selectivity between Si and other materials like photoresist, SiO₂ and Al [23]. It has been seen that as little as 3nm of silicon dioxide is enough to prohibit etching through to the silicon. Smaller holes are then patterned to etch through the thin thermal oxide layer, again using AZ2070 photoresist. The thermal oxide layer is etched through to the device layer with a timed liquid HF etch.

The previously mentioned patterns and the metal contact pad patterns are designed so that after metallisation, the aluminium contact pads overlap the thermally grown oxide layer. This protects the underlying silicon device layer from the final process which etches the sacrificial a-Si layer. This is illustrated in Fig. 2(d). Aluminium contact pads are evaporated onto photolithographically patterned AZ2070 photoresist and subsequently a lift-off procedure is performed overnight using n-methyl-2-pyrrolidinone (NMP) followed by a 2 hour acetone clean at 45°C.

The final stage is then to re-release the nanowire for the final nanowire suspension, this is realised using a highly selective cycled XeF₂ vapour phase etch of the a-Si layer using a Xactix XeF₂ Release Etch System (Fig. 2(e)). 4 etch cycles of 60 seconds at 2.5 Torr etch the 600 nm of a-Si to re-suspend the silicon nanowires without etching the underlying oxidised silicon device layer. Fig. 3 shows SEM images of a fabricated (a) oxidised nanowire and (b) non-oxidised nanowire. This fabrication has been adapted from the work detailed in [24].

Fig. 3: Scanning electron micrographs of (a) oxidised and (b) non-oxidised suspended silicon nanowires with beam width of ~ 42 nm, thickness of ~ 50 nm and lengths (a) 1800 nm and (b) 2000 nm. SEM image (b) is taken at a 60° angle. The fabricated devices have air gaps between the nanowires and side gates ranging between 46 nm and 53 nm.

Beam suspension is verified by a combination of BOX ellipsometry and an observed SEM contrast effect on SOI due to the change in electron mean free path after BOX under-etch. This can be seen in Fig. 3 around the electrode edges which appear lighter than the areas still anchored to the BOX layer. The BOX surface roughness profile, immediately below the beams, is observed to be consistent with the surrounding areas after pull-in. Unsuspended devices are found to have no pull-in occurrence (tested up to $V_{GS} = 100$ V).

3. Results

Electrical characterisation of the suspended silicon nanowires is performed using an Agilent B1500A Semiconductor Device Parameter Analyzer in an air environment at ambient temperature, pressure and humidity. Fig. 4(a) shows electrostatic switch-off of an 1800 nm length oxidised nanowire. The adjoining SEM image (Fig. 4(b)) shows the electrode configuration used during testing. V_{GS} is swept from 0 V to -5 V while V_{DS} is maintained at 0.1 V. The threshold voltage of -1.8 V is observed and electrostatic switch-off shows depletion mode characteristics of the device. At -3.5 V the channel current is 8.56 pA, resulting in an on/off ratio of 10^5 .

Fig. 4: (a) 0 V to -5 V gate voltage sweep illustrating electrostatic switch-off of the source-drain current against a logarithmic drain current axis (main). Gate leakage current and its hysteresis is also measured (inset). Source-drain voltage is held at 0.1 V. (b) SEM image of the device illustrating the electrode configuration.

The highly doped nanowire acts as an always on gated resistor, similar to devices reported in [25]. The current-voltage characteristics of the conducting channel at $V_{GS} = 0$ V can be estimated by

$$I_{DS} \approx q\mu N_D \frac{A}{L} V_{DS} \quad (1)$$

Where I_{DS} is the drain current, q is charge, μ is carrier mobility, N_D is carrier concentration, A is channel cross sectional area, L is length and V_{DS} is drain voltage. At a dopant concentration of $N_D = \sim 1 \times 10^{19} \text{ cm}^{-3}$ and assuming a square 1:1 cross-sectional aspect ratio, the average conducting channel width of the 1800 nm length nanowire in Fig. 4 is calculated to be ~ 10 nm. This suggests the thermal oxide layer thickness averages at 18 nm around the nanowire. This is consistent with ellipsometry measurements performed on exposed device layer sections. Threshold voltage can be estimated by the following linear equation [26]:

$$V_{TH} = \frac{qN_D W}{C_o} + \psi_s \quad (2)$$

Where W is the inversion width, C_o is the capacitance per unit area and ψ_s is the surface potential. This equation predicts under 1 nm inversion at the measured $V_{TH} = -1.8$ V. It is expected that the results seen in the fabricated devices are due to nanowire width variations because of roughness, non-uniform oxidation and likely dopant variance along the channel. The

conduction channel width has been shown to be critical to gate voltage sensitivity [25]. As a result, devices fabricated without a thermal oxide layer show no signs of electrostatic switch-off; measured non-oxidised device characteristics are broadly represented by the following result: I_{DS} is reduced from 183.2 nA at $V_{GS} = 0$ V to ~ 181.8 nA at $V_{GS} = -5$ V with $V_{DS} = 0.1$ V.

Electromechanical pull-in is tested by lateral electrostatic actuation of the suspended nanowires. Single side gate voltage sweeps are applied to devices while maintaining 0 V at all other electrodes. Electrical current readout during and after electromechanical pull-in is shown in Fig. 5(b). The graph shows immediate current flow increase between the gate and the source electrodes at and above $V_{GS} = 39$ V, this is caused by oxide breakdown upon mechanical contact because of the high gate voltage. The current is limited to 30 nA, hence the apparent current ceiling in the graph. Electromechanical pull-in occurs at 39 V, at which point the suspended nanowire's restoring mechanical force is overcome by the actuating electrostatic force. A subsequent conduction path is created between the gate and the source electrode through both thermal oxide layers. The ensuing current leads to joule heating and irrecoverable device destruction. This is shown in the inset of the SEM image of Fig. 5(a). CoventorWare finite element method simulation software is used to calculate the expected electromechanical characteristics of the suspended nanowire. Fig. 6 shows the simulation results for a suspended 50 nm by 50 nm by 1800 nm silicon nanowire pulled in across a 50 nm air gap. A pull-in voltage of 39.125 V is extracted which is very close to the value of 39 V obtained through experiment.

Fig. 5: Electromechanical pull-in test resulting in device destruction after pull-in. (a) The scanning electron micrographs of suspended silicon nanowire show the device before pull-in (main) and after (inset). (b) The graph shows the measured current-voltage behaviour of the suspended silicon nanowire during pull-in. The current is limited to 30 nA. Destruction of the suspended silicon nanowire is due to the high pull-in voltage; a conduction path is formed through the two thermal oxide surface layers leading to joule heating and subsequent device destruction.

Fig. 6: Finite element method simulation of electromechanical pull-in of an 1800 nm length nanowire across a 50 nm air gap is performed using CoventorWare software. Simulated pull-in occurs at 39.125 V. This is very close to the experimentally measured value of 39 V.

Fig. 7 is an SEM image of a 2000 nm length, lightly doped (concentration of $\sim 2 \times 10^{14} \text{ cm}^{-3}$) nanowire. It has been electromechanically actuated to the side gate at $V_{GS} = 35 \text{ V}$ without resulting in device destruction. A trade-off related to source to gate conduction appears to be possible to enable pull-in without device destruction. Further to this, pull-in voltage reduction will be achieved through scaling of nanowire and air gap width. These attributes will be optimised in future devices with modified gate designs and structure sizes to enable doubly clamped NEMS switches which exploit stiction for bistable operation.

Fig. 7: Scanning electron micrograph of suspended silicon nanowire which has been electromechanically pulled in to one of two side gates. Lightly doped configuration remains intact after lateral pull-in to the upper gate.

4. Summary

Suspended silicon nanowires with narrow $\sim 10 \text{ nm}$ conduction channels have been successfully fabricated and characterised. The devices exhibit excellent electrical isolation between the nanowires and the side gates resulting in near-zero gate leakage. The oxidised, suspended silicon nanowires demonstrate depletion mode characteristics upon application of a negative gate voltage with a high on/off ratio of 10^5 . Oxide nanowire surfaces have been made possible by a two stage vapour release fabrication process. Electro-mechanical actuation is observed and strategies for overcoming joule heating induced destruction are considered for future device optimisation towards non-volatile bistable low power transistors.

5. Acknowledgements

This research is conducted under financial support from the EPSRC-JST strategic Japan UK cooperative program NOVTLOS project EP/J000469/1.

6. References

- [1] ITRS 2013 Edition, Emerging Research Devices Chapter (2013)
- [2] Kim, J. H.; Chen, Z. C. Y.; Kwon, S.; Xiang, J., Nano Letters 14 (3), (2014) 1687–1691
- [3] Amponsah, K.; Yoshimizu, N.; Ardanuc, S.; Lal, A., 5th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (2010) 985-988
- [4] Svensson, J.; Lindahl, N.; Yun, H.; Seo, M.; Midtvedt, D.; Tarakanov, Y.; Lindvall, N.; Nerushev, O.; Kinaret, J.; Lee, S.; Campbell, E. E. B. Nano Letters 11 (2011) 3569
- [5] Milaninia, K. M.; Baldo, M. A.; Reina, A.; Kong, Journal of Applied Physics Letters 95 (2009) 183105
- [6] Sun, J.; Wang, W.; Muruganathan, M.; Mizuta, H., Applied Physics Letters 105 (2014) 033103
- [7] Cao, J. ; Vitale, W. A.; Ionescu, A. M., IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS) (2012) 188 – 191
- [8] Feng, X. L.; Matheny, M. H.; Zorman, C. A.; Mehregany, M.; Roukes, M. L., Nano Letters 10 (2010) 2891
- [9] Qian, Y.; Lou, L.; Tsai, M. J.; Lee, C. Applied Physics Letters 100 (2012) 113102.
- [10] Lee, J. O.; Song, Y.-H.; Kim, M.-W.; Kang, M.-H.; Oh, J.-S.; Yang, H.-H.; Yoon, J.-B. Nature Nanotechnology 8 (2013) 36
- [11] Jeon, J.; Pott, V.; Kam, H.; Nathanael, R.; Alon, E.; Liu, T.-J. K. IEEE Electron Device Letters 31 (2010) 371
- [12] Akarvardar, K.; Wong, H. S. P., ECS transactions, vol. 19 (2009) 49-59
- [13] Hinchet, R.; Montes, L.; Bouteloup, G.; Ardila, G.; Parsa, R.; Akarvardar, K.; Howe, R.T.; Wong, H.-S.P., Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (2011) 348-351
- [14] Loh, O. Y.; Espinosa, H. D.; Nature Nanotechnology 7 (2012) 283-295
- [15] Leem, L.; Harris, J. S., Journal of Applied Physics 105 (2009) 07D102
- [16] Nikonov, D.E.; Bourianoff, G.I.; Ghani, T., IEEE Electron Device Letters, vol. 32, no. 8 (2011) 1128-1130
- [17] Onkaraiah, S.; Reyboz, M.; Clermidy, F.; Portal, J.; Bocquet, M.; Muller, C.; Hraziiia, H.; Anghel, C.; Amara, A., IEEE International New Circuits and Systems Conference (2012) 417-420
- [18] Yoon, S. M.; Jung, S. W.; Lee, S. Y.; Park, Y. S.; Yu, B. G., IEEE Electron Device Letters 30(4) (2009) 371-373
- [19] Natsui, M.; Suzuki, D.; Sakimura, N.; Nebashi, R.; Tsuji, Y.; Morioka, A.; Sugibayashi, T.; Miura, S.; Honjo, H.; Kinoshita, K.; Ikeda, S.; Endoh, T.; Ohno, H.; Hanyu, T., IEEE International Solid-State Circuits Conference Digest of Technical Papers (2013) 194-195
- [20] Matsunaga, S.; Hayakawa, J.; Ikeda, S.; Miura, K.; Hasegawa, H.; Endoh, T.; Ohno, H.; Hanyu, T., Applied Physics Express (2008) 091301
- [21] Boodhoo, L.; Yun Peng Lin; Chong, H.M.H.; Tsuchiya, Y.; Hasegawa, T.; Mizuta, H., 8th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (2013) 558-561
- [22] Witvrouw, A.; Du Bois, B. ; De Moor, P. ; Verbist, A.; Van Hoof, C. A.; Bender, H.; Baert, C., Micromachining and Microfabrication Process Technology VI (2000) 130

- [23] Chan, I. W. T.; Brown, K. B.; Lawson, R. P. W.; Robinson, A. M.; Ma, Y.; Strembicke, D., IEEE Canadian Conference on Electrical and Computer Engineering (1999) 1637-1642
- [24] Ghiass, M. A.; Tsuchiya, Y.; Hassani, F. A.; Dupre, C.; Oilier, E.; Cherman, V.; Armini, S.; Bartsch, S.; Tsamados, D; Mizuta, H., 12th IEEE International Conference on Nanotechnology (2012) 1-4
- [25] Colinge, J.; Lee, C. W.; Afzalian, A.; Akhavan, N. D.; Yan, R.; Ferain, I.; Razavi, P.; O'Neill, B.; Blake, A.; White, M.; Kelleher, A. M.; McCarthy, B.; Murphy, R., Nature Nanotechnology (2010) 225-229
- [26] Sze, S. M., Semiconductor devices, physics and technology, John Wiley and Sons, New York, 1985, ISBN: 0471874248