30 Years of electroless plating for semiconductor and polymer micro-systems

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Abstract

Electroless deposition (ELD) is a well-known method for preparing thin films of metals and their alloys. It is a highly selective method allowing additive patterning of isolated and embedded structures on insulating substrates, e.g. glass, plastic or ceramic. It is a relatively low temperature (less than the boiling point of the electrolyte) and low cost process compared to other physical and chemical vapor deposition methods. ELD features uniform and normally conformal deposition (additives may affect its conformality) with low defect density and some unique material properties. In the last 30 years electroless plating of metals (e.g. copper, gold, nickel, cobalt, palladium, iron, silver, etc.) and their alloys, was demonstrated for micro system applications: microelectronics, micro electro mechanics, micro electro optics and microfluidics, micro fuel cells, micro batteries etc. Electroless plating was also demonstrated on nano structures, both artificial and natural. In this paper we present a short tribute to the recent advances in electroless plating in the last 30 years. Those advances and innovations are due to the work of many scientists and engineers on a time span started in the 19th century. The progress in electroless plating followed the need and the trend for better metallization technologies for complex structures with critical dimensions that had been shrinking continuously in the last few decades.

1. Introduction

The title of this review, which is written in 2014, is “30 years of electroless plating”; Electroless plating or deposition (ELP or ELD) had been known and used long before 1984. That technology was used for preparing thin films of metals such as Cu, Co, Ni, Fe, Ag, Sn, Au, Pt, Pd etc., and their alloys. For example, see the review by V. Mandich and G.A. Krulik "50 years of electroless plating of Nickel [1], the book of G.O. Mallory and J.B. Hadju [2], the chapters in books by S.S. Djokić [3] and V. Dubin [4] and in many papers (See for example [5-11]). ELD has progressed in the last 30 years; we have now better understanding of the material properties and there are many new Micro and Nano System Technology (MST and NST) applications. Those achievements are supported by the scientific and engineering research in this field and we should pay tribute to the pioneers and inventors who contributed to the advances in the ELD field in general and to the feasibility of using ELD for micro and nano fabrication in particular. Electroless plating allowed the fabrication of isolated and embedded structures on insulating substrates and entities that cannot be produced by other methods. It allowed the fabrication of isolated metal patterns on plastics, glasses, polymers and organic material. Electroless plating is used also for many other applications, e.g. decoration, metal finishing etc.; however, this paper is dedicated to micro and nano technologies, science and engineering.

Electroless plating, like any technology, has its highlights and problems. Among its useful properties we can count its selectivity and the capability to deposit thin films of metal and alloys on insulators; e.g. glass, ceramics and polymers. It is also very conformal and requires relatively simple deposition tool compared to other metallization techniques. Its problems emerge from the plating bath solution complexity and its nature being an autocatalytic process. ELD solutions are typically more complex than conventional electroplating solutions. ELD uses electrolytes containing few components: metal complex ions, reducing agents, pH adjustment and buffering components and additives which affect both the process and the thin film quality. There are few possible problems: 1) aging of the solution, 2) reaction byproducts affecting the deposition, 3) homogenous nucleation in the volume, 4) nucleation on defects on non-selected regions, and 5) a failure to nucleate on selected regions due to contamination or some other problems with the catalytic surface.

To understand ELD history we should go to the early age of metal deposition that can be dated to prehistoric times. In the paper by L.B. Hunt [12], “The Oldest Metallurgical Handbook- Recipes of a Fourth Century Goldsmith” he mentions that records that bear upon the mining and metallurgy of metals are to be found in occasional passages in the works by Pliny (AD23 – August 25, AD79),

Pedanius Dioscorides (40 – 90AD), Theophrastus (371BC – 287 BC), and Vitruvius (born c. 80 – 70 BC, died after c. 15 BC). Technologies such as soldering and gilding appear in the Leyden Papyrus X from the 4th century [12]. Note that the oldest gilded object known is a copper fragment found in excavations in Ur, currently Iraq, and is estimated to be of the period 3,000 to 4,000 B.C. There are also artifacts that were gold gilded more than 2000 years ago in other places such as China and Japan (S.F. Moran [13]). Even more fascinating is the evidence that methods such as electrochemical replacement plating and flame annealing existed in pre-Columbian culture in South America prior to the 5th century BC (H. Lechtman [14]).

The method of gilding [15] using amalgams had been exploited over the years in spite of its health hazards. That risk probably challenged chemists at the early 19th century to find alternative methods, such as electrochemical deposition. Advances in electrochemistry yielded the various deposition methods that are classified under the definition of electrochemical deposition. Nickel ELD is dated in the modern area to the work of A. Wurtz [16] who describes in 1844 the use of sodium hypophosphite as a reducing agent for nickel plating [17,18]. The term “electroless plating” was originally coined much later by A. Brenner and G. Riddel [10,11] circa 1947. Traditionally, electroless plating was used to deposit metals on insulators, such as glass and plastics [19] for applications such as interconnects and magnetic media applications. In the late part of the 20th century the evolution of electroless plating followed the microelectronics revolution. One should note the major advances in leading research groups, such as at IBM Inc. and Bell Laboratories in the US and NEC Microelectronics Research Laboratories or The Institute of Physical and Chemical Research (RIKEN Institute) in Japan. Advances came also from many other companies such as C. Uyemura & Co., Hitachi Chemical, Victor Corporation of Japan and Sakura G.S.. During the 1980s the critical dimensions of Very Large Scale Integration (VLSI) of Integration Circuits (ICs) crossed the 1 micron scale mark towards sub-micron dimensions and continued shrinking linearly vs. time in semi-log scale coordinates, a trend known as “Moore’s law”. ELD provided viable solutions to many micro and nano scale technology applications, supporting that trend.

The specific demand for selective, conformal and low cost methods was always one of the key factors supporting further electroless deposition research and development. However, it is not trivial as the deposition electrolyte is potentially unstable, it is being depleted during plating, and depends on the substrate catalytic properties. The electroless deposition process itself is rather complex and involves few steps. Modeling of electroless plating includes both the thermodynamic and kinetic considerations.

The thermodynamics principles could be explained [20,21] by the Pourbaix diagrams of the metal/electrolyte and the reducing agent/electrolyte. Such diagrams were constructed for numerous metals and the associated reducing agent. Pourbaix diagram show the regimes where the electroless deposition is possible. Electroless plating depends on the catalytic nature of the substrate and the reducing agent. Detailed list of possible catalytic substrates that can initiate the autocatalytic deposition process appears in the important papers by I. Ohno [2, 22].

Since the solution is potentially unstable, nucleation can occur spontaneously due to local changes in the pH or with the help of the reaction by-products, which may react with the metal ions forming insoluble salts. To stabilize the deposition, preventing homogenous nucleation in the volume, the metal is being complexed with some organic compound, typically organic acids or their salts. Ammonia and amines are also used for making useful metal complexes.

The actual deposition and its kinetics are defined by the following:

1. Transport of the constituents (i.e. metal complexes, reducing agents, other ions, additives) in the electrolyte towards the catalytic surface – by diffusion and/or convection.
2. Adsorption of the constituents onto the surface.
3. Transport, mainly by surface diffusion, of the adsorbed species on the surface.
4. Intermediate reaction involved in the metal complex reduction and decomposition and the adsorbed reducing agent oxidation. Note that there are many possible intermediate reactions and their rates depend on the catalytic seed, as well as on the adsorbed species concentration.
5. Desorption of unreacted species, intermediates and products
6. Transport of the unreacted species, intermediates and products away from the electrode.

Following the initial step of nucleation the metal grows following the deposition reaction as long as there is no significant depletion of any of the electrolyte components or loss of the surface catalytic properties. Understanding those steps has progressed in the last 30 years due to the tremendous advances and proliferation in high-resolution microscopy, material analysis tools, measurement equipment and data processing. Advanced methods such as atomic level resolution imaging or surface probing, sub-nm resolution depth profiling and complex modeling became common. As microelectronics and other micro-technologies proliferated more research was invested on electroless plating, its basics and applications.

Electroless plating deposition tools and associated technologies have also progressed significantly in the last 30 years [23, 24]. Systems for electroless plating are intrinsically simpler than Physical Vapor Deposition (PVD) or Chemical Vapor Deposition (CVD) tools. ELD deposition tools consist mainly of temperature controlled bath, sample (i.e. wafer, package, board etc.) holder, solution handling, sequencing, monitoring and control system and an enclosure with possible ambient control. Critical factor is the temperature accuracy, reproducibility and uniformity over the wafer or board. It is important to eliminate the possibility of hot spot generation leading to local instability and unwanted deposition or deposition on one of the reactor components. In the past, most of the systems were “multi-use”; i.e. the same solution was used for many samples. The solution deposition properties were controlled using a replenishment algorithm. Recently, “single use” systems appeared where the reducing agent is mixed with the stock solution just prior to the deposition on the wafer. Using small amount of electrolyte is useful for high value products where the cost of ownership of the “single-use” electroless plating step is justified.

In this paper we summarize the issues in ELD occurring in the last 30 years. We focus on deposition for micro and nano fabrication as well as deposition on plastics and biology. Those are important fields of use where the specific contribution of electroless plating is meaningful and significant.

2. ELD for interconnects

The best conducting metals for electronics interconnects that can be deposited by ELD using aqueous solutions are copper, silver, and gold. Nickel or cobalt and their alloys, which have much lower conductivity than copper, are also used as diffusion barriers and capping layers. ELD is widely used for packaging and printed circuit boards (PCB) and also been investigated for Very or Ultra Large Scale Integration (VLSI or ULSI) Integrated Circuits (IC) and 3D integration. We focus on copper metallization, since it is the metal of choice for most ELD micro and nano scale interconnect applications. ELD silver and copper alloys with tungsten have also been investigated for “stainless” metal application; however, those alloys’ specific resistivity is higher than that of the pure metal and such alloys can be applied only for low current density or protective coating applications.

Copper was always the metal of choice for conducting electricity on printed circuit boards and since the mid 90s also on chip level. It is being used for delivering electrical power, for ground, for

supplying clock signals and for transferring digital or analog signals between electronic units; both on-chip and intra chip. A summary of recent advances in copper metallization science and technology can be found in numerous papers and in books such those by S. Murarka [25], M. Datta [26] and Y. Shacham-Diamand [27].

2.1. VLSI ICs interconnects

Copper, as the main interconnect conducting material, was proposed already at the 1980s. Few patterning methods had been proposed such as lift-off [28] or the Damascene method [29-32]. Eventually, the Damascene process took over as the dominant copper metallization scheme. Metal deposition onto trenches, followed by chemical mechanical polishing (CMP) became possible due to the seminal effort by researchers at IBM Inc. [33-35].

Electroless plating of copper for VLSI was suggested by P.L. Pay, M. Pauovic and C. Ting already in 1989 [36-39]. The critical dimensions of metal interconnects at that time were not much less than one micron (in mass scale manufacturing), however, 100 nm wide wires with high aspect ratio (> 5) had already been demonstrated in 1991 [40]. This showed the potential of ELD for nano-scale plating, which will be described in further details later in this paper. Following that work numerous recipes for applying copper ELD for VLSI metallization were demonstrated [41-43].

Electroless copper for ULSI metallization was proven to be competitive to electroplating. The resistivity of electroless plated copper was in the range of 2.2-2.3- $\mu\Omega\text{cm}$ and it was capable of forming deep submicron features. Electroless copper plating was highly conformal which was a problem since it created a seam at the center of the interconnect line which had been deposited on narrow trenches. Void-free filling of high aspect ratio via-holes was reported [44-55] with the proper choice of plating additives such as SPS and mercapto alkyl carboxylic acids as accelerator, and PEG-PPG triblock copolymers as inhibitors [48-50]. Void-free electroless copper deposition in sub-micrometer trenches was obtained in the presence of the single poly(ethylene glycol) (PEG) as inhibitor [44, 51] as well as accelerating species such as SPS [52, 53] and its derivatives, 3-N,N-dimethylamino-dithiocarbamoyl-1-propanesulfonic acid (DPS) [54] and 2-mercapto-5-benzimidazole-sulfonic acid (MBIS) [55]. Electroless plating of copper still need further improvements to combine the highest conductivity and the best seamless trench filling compatible with most inter-level dielectric schemes and the process requirements. For example, VLSI interconnects require an alkali-free deposition bath since alkali ions, i.e. Na and K, are major contaminants for the silicon based transistors. Introducing an alkali-free bath solved this problem allowing integration with silicon microelectronics. Another example is the use of

formaldehyde as a reducing agent. This material use is regulated and might be restricted in few countries; therefore, alternative scheme using glyoxilic acid was devised [56]. Typical copper plating bath operates at high pH (> 12.5) and deposition temperature near ~ 70 °C which may be a problem to some polymer based low dielectric insulators. Therefore, other solutions working at lower pH and lower temperatures are also possible, although, they usually yield copper with higher specific resistivity.

2.2. ELD for Barrier and capping layers

Electroless cobalt and nickel alloys can be excellent barrier and capping layers for copper and silver metallization. Electroless cobalt and nickel alloys are highly selective, uniform and serve their function even for ultra thin layers (10-20 nm). To deposit electroless Co or Ni films hypophosphite or dimethyl-amino-borane (DMAB) were used as reducing agents, and as a result of reducing agent oxidation P or B incorporated into the deposit. Furthermore, to improve the thermal stability and diffusion properties, refractory metals such W, Mo, or Re can be co-plated with electroless Co or Ni when the water-soluble compounds of refractory metals were introduced into the plating solutions. For example, tungsten was incorporated into electroless cobalt film up to 12 at.% when tungsten-phosphoric acid was used as a tungsten source in the plating bath. Electroless barriers for on-chip metallization are characterized by the following microstructure effects: a) the so-called “solute effect”, phosphorus (or boron) and tungsten (or Mo, Re) impurities create a “stuffed” boundary, blocking possible copper diffusion through the grain boundaries; b) ϵ -cobalt grains embedded in an amorphous matrix, thus avoiding the high diffusivity paths of the grain boundaries in regular polycrystalline materials.

Regarding VLSI interconnects; barrier and capping ELD had been studied for aluminum metallization that was dominant until the appearance of the copper metallization scheme in the late 80s, early 90s, of the 20th century. Several metal deposition processes were studied for coating the aluminum conductors and filling via holes increasing the reliability of multilevel Al metallization. Selective electroless deposition process was especially appealing because of its selectivity and low cost. Selective electroless metal deposition (Ni, Co, or Pd) with Pd activation was investigated as an alternative to the selective CVD W [57, 58]. In work [59], selective electroless Ni deposition, without any activation step on Al-Si-Cu conductors, was developed for via-hole filling and conductor pattern cladding. It was observed that Ni-Cu(P) overcoat of Al-Si-Cu lines increases corrosion resistance, suppresses hillock formation, and decreases interconnects resistance. The Ni-Cu(P) was selectively

deposited into via holes on Ni-Cu(P) overcoat of Al-Si-Cu lines to obtain a planar surfaces and good contact resistance.

Selectively deposited electroless Ni-P [60] and Co-P, Ni-Co-P [61] films were investigated as the barrier/cladding materials for copper metallization. The former electroless barriers for Cu were effective up to a temperature of 400°C. The introduction of a third alloying element, especially refractory metal, e.g. W, Mo, or Re, improves barrier efficiency. NiB, NiReP and NiWP show ability to serve as a barrier and cladding layers without significant diffusion of copper into the barrier and no Cu line resistance increases at temperatures up to 400 – 500°C. Electroless CoWP thin films showed an ability to function as effective barriers/cladding layers for Cu metallization at temperatures up to 550°C [62]. Electroless barrier layers can be formed on PVD or CVD deposited Co (or Ni) seed layers as well as directly on dielectric layers (such as SiO₂). Self-assembled monolayer of silane-based compounds followed by treatment in a Pd containing activator was utilized as the adhesion promoter/catalytic layer.

SiN or SiC layer are typically used as the etch stop and passivation layer for copper. SiN/Cu or SiC/Cu interface is a major electromigration-voiding site. Selective metal capping with electroless metals was proposed as one of the ultimate solutions to this problem [60-65]. Electroless metal capping/barrier layers such as CoWBP, CoWP, NiMoP [66, 67] also provides barrier properties against copper and oxygen diffusion so that lower effective interconnect capacitance can be obtained with thinner or even without SiN (SiC) layers which have high dielectric constant. It was also demonstrated that both the contact resistance and the leakage that could be lower for a stand-alone electroless metal cap compared to a stand-alone SiN cap, presumably due to the damage associated with the SiN deposition. The electromigration median-time-to-failure (EM MTTF) of damascene copper interconnects with Co capping layer is about ten-times (x10) better than that of Cu metallization with Si(C)N dielectric capping layer. The distribution of the EM failures is also tighter on Co capping wafers (Fig. 1), The increase of the electromigration resistance with an electroless capping layer can be explained by the complete passivation of the top interface as fastest diffusion path resulting in increased adhesion and interfacial bonding strength (i.e. metal/metal > metal/Si > metal/oxygen bonding).

Selective electroless Ni process was demonstrated to fill the contact holes to Si while providing low contact resistance and planar surface [69, 70]. Selective electroless Ni and Co deposition into deep via-contacts etched in silicon (so-called “through silicon vias” or TSV) for 3D interconnects has been also

achieved through the mechanical removal of catalysts from the front surface of the wafers or the use of photosensitive TiO_2 /catalyst process (V. Dubin, private communication). It enables selective TSV filling that eliminates the needs for PVD barrier/seed layer and chemical mechanical polishing that significantly reduces the 3D packaging cost.

2.3. SAM activation

Copper metallization for ultra-large-scale integrated (ULSI) technology has been used as the wiring material replacing aluminum based metallization. Cu has been introduced since it has higher electrical conductivity and higher electromigration resistance compared to aluminum [71]. However, these issues have become critical as interconnect dimensions reached less than 100 nm. There were significant efforts to suppress the dominant mechanisms causing this kind of failure. For example, preventing the occurrence of minute voids, improving the distribution of poly-crystalline orientation and increasing the adhesive strength between Cu wiring and barrier layers [72]. Moreover, Cu metallization may face some other critical failures: 1. Cu is easily oxidized in ambient air, 2. Cu may have severe adhesion problems with many common dielectric thin films in microelectronics, 3. Cu may also transport via inter-level dielectrics, either by diffusion or drift. Especially designed barrier and capping layers are used to overcome those failures. Note that Cu may diffuse via those layers or even react with them causing another kind of failure. The most popular barriers are TaN, TiN, or Ta/TaN bilayer [73]. Alternative barriers are ternary compounds of transition metal films that provide a good copper diffusion barrier due to its nano-crystalline or XRD amorphous structure, such as Ti-Al-N, Ta-Al-N, have been developed using a using a reactive physical vapor deposition (PVD) or chemical deposition (CVD) [74]. It is reported that CVD is preferable for fabricating barrier layer, because disadvantageous characteristics of PVD such as poor step coverage have set critical limits on silicon device applications by increasing the aspect ratio of the trenches [74]. Ruthenium has been also studied as a seedless Cu diffusion barrier. Unfortunately, Ru films exhibit relatively poorer barrier performance that was caused by grain boundaries formation in the film [75]. Lately, RuCr deposited by sputtering [76] or Ru or Ru /TaN layers deposited by atomic layer deposition (ALD) showing good barrier property was reported by Choi [77]. Following those results, it is reasonable to assume that good barriers should have an homogeneous structure with extremely low defect density and structure that reduce or eliminate grain boundary assisted diffusion. For example thin films with stuffed barriers, amorphous films, or nano-crystalline material embedded in an amorphous phase

As mentioned above, electroless deposition also has superior advantage due to their simplicity and by having a better step coverage on complex shape substrate. The electroless NiB, CoB, CoW-X (X=P, B), CoSnB, Pd films have superior thermal stability as a capping layer or barrier layer [78-83]. Moreover, the insertion of a self-assembled-monolayer (SAM) to the formation of these layers is effective to produce conformal and thin film [84-87].

Self-assembled monolayers, comprised of molecules as short as ~2 nm, has been investigated as diffusion barrier [88]. An interesting approach was integrating all the various wet processes together onto a unified process, including barrier layer, copper interconnects metallization, and capping layer formation. A proposed “all wet” process [84] is shown in Fig. 2 where the organosilane layer was formed on a sulfuric peroxide mixture solution (SPM) activated SiO₂ substrate by wet-chemical method. The alkoxy group in the silane radical makes a strong bond with the SiO₂ surface, and the amino group of the reverse position traps the palladium catalysts initiating the electroless deposition, resulting in the formation of the diffusion barrier layer. Electroless NiP, NiReP, and NiB films are uniformly deposited by using 3-aminopropyltriethoxysilane (APTES) as the organosilane molecule. Because SAMs could provide the formation of minute Pd nuclei less than 2 nm with a high density [89]. This all-wet process has also been applied to low dielectric constant (low-*k*) materials [90,91]. CoWP film exhibit excellent barrier properties against Cu, however, it was difficult to form a thin CoWP layer on the SiO₂ surface. Therefore, in some cases an electroless bilayer, such as CoWP/NiB is used. An evaluation of sheet resistance measurements suggested that the CoWP/NiB film shows appropriate barrier properties for Cu diffusion up to 400 °C and trenches 100 nm wide were coated with a 10 nm CoWP/NiB barrier followed by successful trench filling by electroless deposition of Cu [92,93].

SAM activated electroless plating can be also applied for additive nano-scale patterning. In this case the high selectivity of the electroless plating process is being utilized. The SAM can be applied by Scanning Probe Lithography (SPL) either as etch or deposition resist material or as a catalytic material. Using SPL of SAMs is a promising method because of its high-resolution and also imaging capability. Additionally the high resolution position definition allows nanometer scale alignment accuracy and a potential for the manipulation [94,95]. Combining SAM patterning by SPL with electroless plating will allow writing nano-scale metal and allow nano wires with high positioning accuracy.

2.4. Gold electroless plating

The growing need for high quality packaging promoted special advances in electroless gold plating. A review of this issue is summarized in the paper by T. Okinaka “Some Recent Topics in Gold Plating for Electronics Applications” from 1998 [96]. This work and others by the group at Waseda University, Tokyo, Japan, demonstrated numerous electroless gold bath chemistries for both soft and hard gold applications. The research on gold electroless plating is still ongoing supporting the need for gold finish for electronic packaging methods such as aluminum or gold wire bonding or surface mount technology (SMT).

3. Electroless plating for micro magnetism

The field of micro magnetic devices progressed rapidly in the last 30 years following advances in lithography as well as in thin film deposition and characterization. We will describe here the advances in magnetic recordings, hard disk drives, as they are known. Hard disk drive technology has always been a key information technology. Magnetic memories today have become more important than ever due to the growth in the Internet and network computing, also known as cloud computing. The magnetic materials and other supporting metals can be deposited by physical vapor deposition (PVD), i.e. sputtering or by electrochemical deposition. Electroless Deposition (ELD) has also played a role in developing magnetic devices and will be described here.

Electrodeposited CoNiFe ternary alloys, with high saturation magnetic flux density (B_s), over 2.0 T [97], are important materials for write-head cores of perpendicular magnetic recording system. Electroless deposition is also an attracting method for preparing uniform ferromagnetic films on substrates with fine and complex geometries that can be used for magnetic recording as well as to other applications, such as magnetic solid-state memories or magnetic sensors,. For example, the “proximity switches”, using electroless NiFeB [98] as a magnetic flux inducing film, improved the performance regarding the detection distance. Such components are widely used with market share > 50% and total sales of \$135M in 2014.

When a magnetic field is applied to ferromagnetic materials, they are magnetized along the direction of the applied field and retain magnetization after removal of the field. In order to reduce this residual magnetization, B_r , to zero, a reverse field equal to coercivity, H_c , is required. The ferromagnetic material can be divided into soft and hard magnetic materials according to the value of H_c . Note that the useful value of H_c depends on the application. For example, for magnetic recording,

the requirements for the soft magnetic materials are $H_c < 1$ Oe and high saturation magnetic flux density, B_s . For the same application the requirements for the hard magnetic material are $H_c > 1000$ Oe with controlling magnetic easy axis. The composition vs. B_s diagram for ferromagnetic metals of Co-Ni-Fe bulk ternary alloy published by Bozorth [99]. Many high B_s materials (or high M_s materials) with composition near $\text{Fe}_{60}\text{Co}_{40}$ are known. Generally, the B_s values are related to the composition, however, the value of H_c depends strongly on the material design and the manufacturing process. In the following section we provide more information about electroless deposition of hard and soft magnetic materials for magnetic recording.

3.1 Hard magnetic films [100]

The application of electroless Co film to magnetic recording media was first proposed by Fisher and Chilton in 1962 [101] and a large number of studies were done during the 1960s, focusing on the correlation between plating conditions and film properties [102]. The plated films were applied to magnetic drums and analog disks in the 1970s and to the high-density storage system of PATTY (Packaged air-tight tiny disk) by NTT in 1981. Electroless CoNiP media, as well as sputtered $\gamma\text{-Fe}_2\text{O}_3$ media, were utilized. Subsequently, various plated disk systems have been shipped and precision production technology established. These films were developed for the longitudinal recording system.

A higher recording density can be achieved by decreasing medium thickness and by increasing H_c in the case of the longitudinal recording system. However, the former also decreases the total magnetization of the medium and the latter causes saturation of the recording head. Moreover, it was observed that the reproduced voltage in the higher recording density region decreases rapidly with an increase in recording current. Iwasaki et al. confirmed that such a decrease in reproduced voltage is due to the formation of a circular mode of magnetization [103]. They also found that such a circular mode of magnetization could be transformed to a perpendicular mode, recovering the reproduced voltage, and finally, they proposed a perpendicular magnetic recording system.

The research on electroless-deposited perpendicular magnetic recording media started with CoWP films [104,105] with the c -axis perpendicularly oriented hcp structure. The crystal orientation and magnetic properties were continuously improved by adding other elements such as Mn to the alloy systems, and CoMnP, CoNiMnP films were developed [106]. Co-deposition of Mn induced strong c -axis orientation of hcp Co, which resulted in large anisotropy energy, H_k , and coercivity, H_c , although the Mn content in deposits was very small in these films. By employing the CoNiMnP rigid disk medium, it was first confirmed that perpendicular magnetic recording could be achieved by

electroless-deposited media [106]. Subsequently, the element of Re was added to the CoNiMnP, and the CoNiReMnP films were developed [107]. Co-deposition of Re lowers M_s and thus reduces the demagnetizing field $4\pi M_s$ without destroying the crystal structure of the c -axis perpendicularly oriented hcp crystallite. It has been suggested that the complexant plays an important role in controlling the codeposition of Mn or Re and the film properties [108]. Addition of tartronic acid as a mixed-complexant causes perpendicular orientation of the c -axis of hcp Co instead of Mn codeposition. Thus, CoNiReP films without Mn addition were developed and demonstrated excellent properties [109].

Electroless NiP film [110] has been demonstrated for perpendicular magnetic recording media with aluminum disk competing with vacuum deposition processes. Electroless deposition attracts attention again for producing a bit patterned media (BPM) with the areal density of Tera bit per inch². BPM is ordered arrays of ferromagnetic nanodots, T. Homma's group in Waseda University, Tokyo, Japan, used an electroless deposition process for fabricating CoNiP nanodot arrays (less than 50 nm in height) with high magnetic coercivity of over 3000 Oe. They improved the crystallinity of the CoNiP deposits in the initial deposition stage by applying an fcc-Cu(111) underlayer with low lattice mismatch to hcp-Co(0002), and an autocatalytic electroless deposition process at the Cu surface was carried out by using dual reducing agents, H_2PO_2^- and N_2H_4 [111,112]. Moreover, they studied the behavior of reductants adsorbed to the Cu surface by plasmon antenna enhanced Raman scattering and modeled this effect by Density Functional Theory (DFT) calculation [113].

3.2. *Soft magnetic films*

We summarized our developed soft magnetic film produced by electroless or electrodeposition method in table 1. The key for lowering coercivity of soft magnetic would be change the film crystallinity to nano-crystalline [114]. Co-deposition of B or P originated from reducing agent into magnetic film assist the production of nano-crystalline. Co-deposition of B or P, whose origin is from reducing agent, into the magnetic film assists the production of nano-crystalline film. However, the co-deposition reduces the B_s of films produced by electroless deposition. Nevertheless, the electroless deposition can provide other soft magnetic properties comparable to those of films made by electrodeposition.

Electroless deposition could provide the soft magnetic film with no magnetic boundaries. The group of Waseda University investigated the possibility of the application of Co–Ni–Fe-based alloy thin films electroless-deposited on a disk substrate to the SUL [115]. The electroless-depositing the SULs

of a Co–Ni–Fe–P or Co–Ni–Fe–B alloy without marked macroscopic magnetic domain boundaries [116,117]. Fig. 3 shows magnetic domain images observed through the Kerr effect for the Co–Ni–Fe–P SULs, which were prepared without and with the applied magnetic field of ca. 800 Oe during electroless-deposition, respectively. The magnetic field was applied in the fixed direction parallel to the disk substrate while the disk substrate was rotated concentrically. The Co–Ni–Fe–P SUL deposited without the magnetic field does show clear and complicated magnetic domain boundaries, whereas, the SUL deposited with the magnetic field has no marked domain boundaries. In addition, the magnetic domain boundaries of the former were readily moved when an external magnetic field was applied, therefore, the domain boundaries cause the spike noise. On the other hand, no domain boundaries were induced in the latter even when the external magnetic field was applied.

4. ELD for Micro Mechanical Systems

Electroless plating has been intensively investigated for micro electro mechanical systems (MEMS). Electroless plating offers unique properties for MEMS such as: selective deposition on very high aspect ratio features and onto very deep trenches, unique compositions, low temperature processing and low stress films. Electroless plating was derived mainly for electrostatic actuators; however the option to deposit magnetic materials has also been investigated. Similar to VLSI and packaging, electroless plating can be used for conducting layers, barriers, and corrosion protection layers. Electroless plating is mostly suitable for thin films, with thickness of few nanometers to few microns.

Electroless plating for MEMS was demonstrated over a broad spectrum of applications: actuators, sensors, micro-machined fuel cells, micro batteries and more. The common denominator for all those applications was taking advantage of the highlights of electroless plating: i.e. selectivity, conformity, high aspect ratio deposition and relatively low cost.

In addition to the common use for interconnect deposition; electroless plating is also used for electrode materials for sensors and structural material for MEMS actuators. Typically Au, Ni, or Pd [119-121] are used as various components for electrochemical sensors. ELD is also a simple method that can be used, for example, for sensor backside contact application[122].

ELD was also employed for MEMS actuators [123, 124]. Common structures are shown in figure 4. It can be used as capping layer over micro-machined suspended beams, lowering the electrical resistance of the structure (Fig. 4, left). It can be embedded onto polymers or suspended in air (Fig. 4 center and right). Electroless plating was demonstrated for both electrostatic driven MEMS actuators

and for magnetic MEMS actuators [125-128] and for other micro-machined devices such as batteries [129] or fuel cells [130].

5. ELD and nano technologies

Nano technologies are defined as technologies with critical dimensions in the nano-meter scale range. It refers to both “top down” and “bottom up” approaches; i.e. to conventional downscaling of micro-technologies or the buildup of larger units from nano-meter scale structures. Electroless deposition was considered as one of the candidates for metallization of nano-scale features of both approaches. An excellent summary was published by A. Bittner in 2009 [131]. One important use of electroless plating is its application for nano-scale contacts. Making good contacts is critical for electrical activated nanostructures or nano-components that generate electrical signal or power. Therefore, electroless plating can be used to selectively deposit nano-wires on pre-determined features interfacing nano-scale devices (Fig. 5)

For “top down” metallization, mainly for ULSI ICs the main problem is the realization of high aspect ratio nano-scale, less than 50 nm wide conductors for CMOS ICs interconnect and contacts in 2014. The Narrow Line Resistivity Increase (NRLI) effect [132] requires very thin barrier and capping layers; with few nanometer thickness. Alloys of Ni and Co with refractory metals such as tungsten or rhenium yield good barrier and capping layers that can be uniformly and secretively deposited over large areas [132]. Those films contain also boron, phosphorous or both. The material properties of Co alloy films have been intensively studied by A. Kohn [133-135] and T. Osaka [136,137]. They showed that those alloys could be deposited as very thin layers made of a Co nano-crystals embedded in an amorphous Co alloy matrix.

ELD on nanostructures

Metal and metal-oxide nanotubes are in the spotlight for a wide range of applications, such as selective chemical and biological sensors, lithium ion secondary batteries, dye-sensitized solar cells and photo-catalysts [138]. Metallic tubes, synthesized by a polymer-based template approach using electroless deposition, were demonstrated by a group at State University of New York at Binghamton [139]. They deposited gold, copper, and nickel by electroless deposition as thin shell films on sub-micrometer polymer fibers, and after thermal degradation of the template fibers at 300 and 650 °C, tubes between 450 and 730 nm were obtained with wall thicknesses of 50–150 nm. The group of

Yamaguchi University, Japan also succeeds in the preparation of micrometer-sized bismuth, nickel oxide tubes by combining technique and electroless deposition method [140].

The template-synthesis of mesoporous silica through self-assembly of surfactants which has the pore diameter of 2–50 nm have also attracted increasing interest for many applications [141]. The highly ordered mesostructured Ni and Co particles are formed by metal deposition in the aqueous domains of lyotropic liquid crystals (LLC) using different reducing agents of electroless deposition [142].

An interesting technology under investigation for flexible electronics is the electroless deposition of Zinc-Oxide [143]. It can be deposited as a meso-porous materials and it was recently demonstrated to be suitable for integration with Low Temperature Poly Silicon (PLTPS) Extended Gate Ion-Sensitive Field Effect This Film Transistor (IS-TFT) [144] forming a flexible sensor.

Regarding “bottom up” technologies, electroless based metallization on biological templates was developed and demonstrated by many research groups. For example is the fabrication of nanowires from microtubules [145-150], viral envelopes [151-156], DNA [157,158], amyloid fibers [159,160], S layers [142] and actin [161]. Electroless deposition was initiated by either palladium or platinum nano-cluster seed [145-153] or by catalytic metal (i.e. Au, Ag, Ni etc.) nano particles [160,161]. Following nucleation the metal continues to grow by electroless plating.

Electroless metal was also deposited on microorganisms [162]. In that specific work the deposition bath conditions led to the loss of the cells' viability and the metallized cells were used only as magnetic particles and not as a biologically active material. Another work is the metal coatings of microorganisms using Au nanoparticles highly selective deposition on bacteria surface [163]. A standard assay of PI/SYTO 9 dye was used to confirm that the bacteria survived the complete fabrication process retaining its viability. Another example is the use of the positively charged antiseptic reagent cetyltrimethylammonium bromide (CTAB) for nanoparticle coating of nanostructures on gram-positive bacterium, such as *Bacillus cereus*. In that case, nanoparticle deposition was driven by the electrostatic interaction between the negatively charged teichoic acid on the bacteria and the positively charged CTAB molecules on the surface of the 45 nm diameter Au nanoparticles.

Directed silver ELD on the surface of soluble enzyme molecules (Fig. 6) with preserved activity was demonstrated [132,164,165]. Selective silver metallization of soluble enzyme molecule enabled

constructing very thin coating, with the retention of the enzyme biological activity and solubility. Reducing agent was attached to the surface of soluble glucose oxidase molecules. Addition of metal ions leads to metal nucleation and growth on the enzyme. This process results in an electrical conductor laying close to the catalytic site of the enzyme without blocking it to substrate access. Thus a metal/Glucose Oxidase (GOX) was formed retaining the enzyme activity. The enzymatically active silver-glucose oxidase hybrids may provide a new simple method for glucose biosensor fabrication. This sensor operated also in the absence of oxygen, assuming that the deposited silver on the enzyme's surface acts as an effective nano-wiring.

6. Summary and conclusions

Electroless plating has progressed dramatically in the last 30 years. The main factor was the need for thinner films, better uniformity, improved defect density and the compatibility to the advances in micro and nano fabrication. Innovations in electroless plating emerged in the last 30 years: better catalysis using self-assembled monolayers [136,137], electroless atomic layer deposition by the group of Prof. J.L. Stickney [167]) and nano-scale deposition on nano-tubes [131] and proteins [164,165,166]. In this review we focus on deposition from an aqueous solution; however, it is also possible to deposit from ionic Liquids. The question now is where and what are the next challenges of electroless plating where there is an advantage for low cost, rapid and highly selective deposition method in insulators.

There are few growing micro and nano technologies that can benefit from advances of electroless plating: a. Functional printing: 2D, 2.5D and full 3D, b. Flexible electronics, c. Display technology, and d. Wearable electronics and the “Internet of things” (IoT).

Recent advances in printing are being used now for additive manufacturing of components on demand. It is a possible paradigm shift that has the potential to change the industrial landscape. Manufacturing will drift to small and medium enterprises that could print products on demand. It is even seems possible to conceive at-home manufacturing of products such as toys or home tools. Additive manufacturing requires new tools and materials. Additive manufacturing allows cost effective production at medium and small quantities; eliminating the advantage of high volume manufacturing. However, additive manufacturing is still not cost effective and its material selection is limited. There is a dire need to develop new functional “inks” that will provide wide material selection in addition to insulators; i.e. semiconductors, conductors, piezoelectric, magnetic etc. There is a significant progress in 2D printing using methods such as ink-jet, gravure or laser induced printing. However, all 3D printing tools today use plastics that are insulators. Even future use of conducting polymers that can be

3D printed or conductive inks for 2D printing provide a limited solution since the conductivity of those materials is a fraction of the same materials deposited by thin film technologies (i.e. CVD, PVD, and plating). A potential solution is to use electroless plating on printed seed as way to achieve high conductivity on printed substrate. Feasibility proof exists; metals have already been deposited by electroless plating on polymers that are used for 3D printing or in printed seed.

Flexible electronics and display technology are also growing fields. The increased demand for mobile devices and systems is driven by the growing Internet and communication technologies. The critical line width of thin film transistors and interconnects for display is almost two orders of magnitude larger than that of the leading ULSI circuits. This open new opportunities for electroless plating and self-aligned processes which save masking step and do not compete with high quality, though more expensive, vacuum systems that are used for Integrated Circuits (IC) manufacturing.

Last, but not least, is the growing trend of the Internet of things (IoT). It requires a lot of sensors that will feed information to the network. Printed sensors for wearable devices are one way to link the end user, either human or a system, to the net. This technology is related to the existing Radio Frequency Identification Devices (RFID), though it adds another dimension when it is integrated with sensors: chemical, bio-chemical, and physical (i.e. temperature, humidity, pressure, acceleration, etc.). Electroless plating of the sensor electrodes and interconnects is one way to reduce cost. Linking this with printing technology can even reduce cost and allow point-of-care manufacturing saving time and reduce logistical infrastructure.

In addition to that foreseeable applications and growing fields we anticipate new innovations in few other fields. Some have been demonstrated, such as electroless plating in nano-scale biotechnology for nano-interconnects or nano-gaps; and some are yet to be discovered.

Acknowledgements

In summary of the last 30 years one should pay tribute to the individuals and groups who contributed to the field of electroless plating along those years. We should pay tribute to prominent scientists such as Prof. Hideo Honma from the Faculty of Engineering, Kanto Gakuin University, Japan, Prof. Mordechai Schlesinger from University of Windsor, Windsor, ON, Canada, Prof. Paul A. Kohl from School of Chemical Engineering, Georgia Institute of Technology, Atlanta, Georgia, USA, and Prof. Izumi Ohno from the Tokyo Institute of Technology, Tokyo, Japan, Dr. Madhav Datta from Cooligy Precision Cooling, Emerson Network Power California, USA. We also pay tribute to the IBM

researchers, Dr. L.T. Romankiw, Dr. P. Bindra, Dr. C. Sambucetti, Dr. Milan Paunovic and other distinguished researchers who contributed so much to the field of electroless plating allowing the great advances in the last 30 years as we humbly tried to present here. Their research was summarized in the IBM Journal of research and development seminal Volume 28, Number 6, Page 690 (1984) - Materials/Packaging.

Thanks to the students and post docs of Prof. Shacham-Diamand and Prof. Osaka. Also thanks to our colleagues at Tel Aviv University and Waseda University, especially Prof. E. Gileadi, Prof. J. Rishpon, Prof. T. Homma, Prof. T. Momma, Prof. A. Inberg, and Prof. A. Freeman. Our gratitude to Ms. Yelena Sverdlov, senior chemist and electroless plating lab manager at Tel Aviv University who is responsible to many Co, Ni and Cu alloy plating recipes. Thanks to our friends in Tower/Jazz Inc., especially to Ms. Shternfeld-lavie Zmira, for technical support.

Thanks also to the various funding agencies that funded our research along the last 40 years;. In the USA the SRC, in Israel the Israeli Infrastructure foundation at the ministry of science and the MAGNET program of the ministry of economy, and in Japan MITI and JST. Val Dubin acknowledges the NSF for partial support of his work on electroless Cu and Co (SBIR Phase I Award: IIP – 1315056).

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List of figures and tables

Figure 1. Damascene copper interconnect electromigration data comparing undoped copper with cobalt alloy capping layer to Si(C)N dielectric capping layer.

Figure 2. Schematic illustrations of SAM formation and functionalization processes

Figure 3. Magnetic domain images observed through the Kerr effect of Co–Ni–Fe–P soft magnetic underlayer on a disk substrate electroless-deposited (a) without and (b) with an external applied magnetic field. The thickness of each sample is 1 μm . [118].

Figure 4: Selective deposition of various options for electroless deposition for MEMS applications: Metal cap on suspended beams (Left), embedded into flexible material (Center) and suspended metal beams released over solid substrate (right).

Figure 5: Schematics of ELD on a nanoscale object (dark) and of “wiring up” the object by ELD Sensitization by metal M1 (gray), deposition of metal M (dark gray) by the reductant RH [131].

Figure 6: Two modes of generating low load (A) and high load (B) of silver-reducing moieties on glycoprotein surface [165].

Table 1: Electric, magnetic properties for film produced by electrodeposition or electroless deposition

Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Table 1: Electric, magnetic properties for film produced by electro-deposition or electroless deposition

* Indicates ELD, other entries
are by electro-deposition

Alloy	B_s / T	H_c /e	μ / -	$\rho/10^{-6}\Omega\text{m}$	$10^{-6}\times\lambda$ / -	Crystalline structure
80-NiFe	1.0	< 0.5	1000 ~ 3000	20	Nearly zero	fcc
45-NiFe	1.4 ~ 1.6	< 0.5	1000 ~ 2000	40 ~ 50	+ 10 ~ + 20	fcc
NiFeMo ¹⁾	0.7	0.06	6700	40	-	fcc
NiFe ²⁾	1.0	1.8	1300	56	-	fcc
CoNiFeS ³⁾	1.7	1.0	650	50	+ 4.4	fcc
CoNiFe ⁴⁾	2.1	1.2	650	25	+ 1.8	fcc + bcc
CoFe ⁵⁾	2.4	5	-	-	-	bcc
FeP ⁶⁾	1.4 ~ 1.6	0.2	1400	110	+ 27	amorphous
NiFePC ⁷⁾	1.2	1.8	-	170	+ 7.5	amorphous
*CoB ^{8,9)}	1.45	0.7	400	-	- 1.0	hcp
*CoFeB ^{9,10)}	1.6 ~ 1.8	0.7	650	30	+ 5.6	fcc
*NiFeB ^{9,11)}	1.0	0.5	1000	40	+ 5.0	fcc
*CoNiFeB ¹²⁾	1.75	3	700	70 ~ 90		bcc
*CoNiFeB ¹³⁾	2.0	20	-	-	-	bcc

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