An Accurate Model for Predicting High Frequency Noise of Nanoscale NMOS SOI Transistors

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Abstract—A nonlinear and scalable model suitable for predicting high frequency noise of N-type Metal Oxide Semiconductor (NMOS) transistors is presented. The model is developed for a commercial 45 nm CMOS SOI technology and its accuracy is validated through comparison with measured performance of a microwave low noise amplifier. The model employs the virtual source nonlinear core and adds parasitic elements to accurately simulate the RF behavior of multi-finger NMOS transistors up to 40 GHz. For the first time, the traditional long-channel thermal noise model is supplemented with an injection noise model to accurately represent the noise behavior of these short-channel transistors up to 26 GHz. The developed model is simple and easy to extract, yet very accurate.

Index Terms— CMOS, High Frequency Model, Microwave Frequency, Noise, Large-Signal, Silicon on Insulator (SOI).

I. INTRODUCTION

NANOSCALE complementary metal oxide semiconductor (CMOS) technology is an excellent platform for implementing single-chip systems [1]. Cutoff frequency f_T and maximum oscillation frequency f_{MAX} of advanced CMOS transistors have surpassed 200 GHz mark, enabling microwave and mm-wave applications [2]. Implementing such circuits with first time success remains elusive due to limited accuracy of the available device models on conductive Si substrates. Accordingly, comprehensive deep sub-100 nm CMOS models that accurately capture DC, RF and noise characteristics of transistors are of great demand. To this end, several MOSFET models have already been developed [3–9].

Most existing MOSFET noise models are based completely upon thermal noise, assuming that the noise originates from several thermal noise sources including a finite channel conductance, induced gate noise correlated to the channel noise, and various parasitic resistances [10–17]. To help explain the noise behavior (and also high frequency and high power behavior), a distributed gate resistance effect has been introduced for multi-finger transistors. Due to difficulty in its implementation, instead of using a lumped RC model, this effect has been most commonly modeled by a lumped gate resistor with a modified empirical resistance value [18–20].

Despite various modifications to capture the noise of nanoscale transistors, the classical long-channel thermal noise model requires geometry and bias dependent empirical parameters, especially when the channel length scales down below 100 nm.

A shot noise model has been proposed for ultra short-channel MOS transistors with ballistic transport, where the shot noise is due to electron injection from the source region through the potential barrier and into the channel [21]. In such ballistic transistors, the channel thermal noise can be ignored. While this shot noise model fits the noise behavior of ultra short-channel transistors investigated by device simulation, the model is not experimentally verified as no comparison to measured noise data has been reported. Additionally, current sub-100 nm MOS transistors are still semi-ballistic transport devices and the aforementioned shot noise model is not expected to completely capture their noise behavior. In this work, a combined shot-thermal channel noise model, which integrates the classical long-channel thermal noise model and the shot noise model is proposed to accurately predict the noise behavior of the semi-ballistic transport MOS transistors up to 26 GHz.

II. VIRTUAL SOURCE (VS) BASED DC MODELING

As the channel length becomes comparable to the electron mean free path in the channel, the classical drift-diffusion transport model fails [22]. By employing only ten physical and empirical parameters, the semi-empirical Virtual Source (VS) model captures the characteristics of modern short channel MOS transistors to a good accuracy. In this model, the normalized drain current I_d/W is calculated as the product of channel charge areal density Q_{x_0} , virtual source velocity v_{x_0} at the top of the energy barrier near the source, where the gradual channel approximation applies [4], and an empirical smoothing function

$$\frac{I_{ds}}{W} = Q_i(x_0) v_{x_0} F_{sat}, \quad (1)$$

$$F_{sat} = \frac{V_{ds}/V_{dsat}}{\left(1 + (V_{ds}/V_{dsat})^\beta\right)^{1/\beta}} \quad (2)$$

TABLE I
EXTRACTED VS PARAMETERS

Parameters	NMOS	Notes
L_g (nm)	40	Channel length
L_{ov} (nm)	12	Total overlap channel length
C_g ($\mu\text{F}/\text{cm}^2$)	2.625	Gate capacitance
R_s (Ω - μm)	153	Series contact resistance
$DIBL$ (mV/V)	156	Drain-induced barrier lowering
SS (mV/dec)	97	Subthreshold swing
v_{xo} (cm/s)	$9.1\text{e}6$	Electron velocity at virtual source
μ ($\text{cm}^2/\text{V}\cdot\text{s}$)	144	Mobility
α	3.5	Fitting parameter
β	1.8	Fitting parameter

TABLE II
EXTRACTED EXTRINSIC PARASITIC ELEMENTS

Width (μm)	42	84	168	336
C_{pg} (fF)*			13.65	
C_{pd} (fF)*			12.11	
L_g (pH)	32.13	30.33	35.32	35.41
L_d (pH)	32.24	23.37	31.55	35.72
L_s (pH)	45.22	41.26	39.76	38.40
R_g (Ω)	25.78	14.15	5.9	2.95
R_d (Ω)	2.62	2.47	2.01	2.08
R_s (Ω)	0.36	0.34	0.69	0.85

* C_{pg} and C_{pd} are extracted from an open de-embedding structure.

β is an empirical parameter to be fitted to the nonlinear dc measurement. The VS parameter values for the NMOS transistors investigated in this work are extracted from the dc behavior and are listed in Table 1. Reference [4] provides detailed information about the VS model parameters.

III. LARGE SIGNAL RF MODELING

A simple equivalent circuit based MOSFET RF model has been developed for NMOS transistors in this technology as shown in Fig. 1 (a). It consists of the core nonlinear VS model, intrinsic parasitic capacitances C_{gs} , C_{gd} , C_{ds} (enclosed by the blue box in Fig. 2) and extrinsic parasitic elements (C_{pg} , C_{pd} , L_g , R_g , L_d , R_d , L_s , R_s) originated from interconnections, vertical interconnects (VIAs), RF pads and transistor layout parasitics. All these parasitic elements have been extracted from the measured S-parameter data. The measured transistors have multi-finger layout with $1\text{ }\mu\text{m}$ finger width and 40 nm effective finger length and number of fingers ranging from 42 to 336. The S-parameters were measured up to 40 GHz using Keysight E8361A PNA with INFINITI GSG RF probes. Moreover, the de-embedding patterns were measured and used to eliminate the parasitic elements associated with the pads.

The extrinsic parasitic elements should be accurately extracted prior to the extraction of intrinsic parasitic elements. The gate and drain parallel capacitances are extracted from an open de-embedding pattern that is fabricated on the same chip. Next, extrinsic parasitic inductances and resistances are extracted. Various extraction techniques have been developed for different technologies [23–26]. Among them, techniques presented in [23] and [24] have been found to be most effective for this short-channel CMOS SOI technology. Under cold bias condition ($V_{ds} = 0\text{ V}$ and $I_{ds} = 0\text{ A}$), the transistor operates in the

Fig. 1. Large signal equivalent circuit model of NMOS transistors under (a) normal operation and (b) cold bias condition. The DC characteristics is given by VS model (inside the red box). Elements inside the blue box are denoted as intrinsic elements whereas those outside of the box are extrinsic elements.

Fig. 2. Frequency dependence of the extracted intrinsic elements, C_{gs} , C_{ds} , C_{gd} , R_{ds} , and g_m for a $42\text{ }\mu\text{m}$ size transistor biased at $V_{gs} = 0.9\text{ V}$, $V_{ds} = 0.9\text{ V}$.

linear regime and the equivalent circuit of the transistor simplifies to the one shown in Fig. 1 (b). During the extraction of extrinsic parameters, reference [24] utilized the fact that channel conductance in the linear regime is proportional to the overdrive voltage ($V_{gs} - V_t$). This assumption has been verified for the NMOS transistors investigated in this work. By utilizing Z-parameters and equations developed in [24], all series parasitic elements may be extracted with a simple linear regression (see Table 2). Note that gate resistance R_g is dominated by poly-silicon resistance, thus scales with transistor width as shown in Table 2. Drain and source parasitic resistances R_d and R_s on the other hand, are mainly due to contact and access resistances, which may be why they show weak dependences to the transistor width.

From the equivalent circuit model, the intrinsic parameters were extracted from intrinsic Y-parameters, which can be calculated from the measured S-parameter with the extrinsic parasitic elements subtracted. Fig. 2 depicts extracted intrinsic elements vs. frequency for a $42\text{ }\mu\text{m}$ wide transistor (42 fingers with finger width of $1\text{ }\mu\text{m}$) biased at $V_{gs} = 0.9\text{ V}$, and $V_{ds} = 0.9\text{ V}$. The fact that these intrinsic elements are constant over a broad frequency range indicates the physical accuracy of the model. The same extraction technique has been applied to transistors with different sizes ($84\text{ }\mu\text{m}$, $168\text{ }\mu\text{m}$, and $336\text{ }\mu\text{m}$ wide NMOS

Fig. 3. Accuracy of the VS model demonstrated by comparison to the extracted intrinsic parameters: (a) g_m and (b) R_{ds} for different bias conditions for an 84 μm wide transistor. Extracted intrinsic parameters g_m and R_{ds} are tossed out in favor of the scalable VS model.

transistors) under different biasing conditions. The close match between the extracted transconductance g_m and dI_d/dV_{gs} of the VS model and between the extracted R_{ds} and the reciprocal of dI_d/dV_{ds} from the VS model, as shown in Fig. 3, is yet another proof of the accuracy of the VS model.

IV. NOISE BEHAVIOR OF NANOMETER SCALE TRANSISTORS

According to classical high frequency noise models, the noise sources in a MOS transistor originate from thermal noise associated with access resistances and channel resistance as shown in Fig. 4(a). For the gate noise $\overline{i_G^2}$, in addition to the thermal gate noise stemmed from the physical gate resistance, an induced gate noise is introduced to the classical model of sub-micron MOS transistors to capture the noise due to coupling between the potential fluctuations in the channel and the overlaying gate through gate-oxide capacitance [27]. On the other hand, channel thermal noise is given by $\overline{i_{Ch}^2} = 4g_k T g_0$, where g_0 is the output conductance at $V_{ds} = 0$ V (linear region) [10]. Parameter γ is the so-called channel noise parameter, equal to 2/3 in saturation and 1 in linear regime for long channel

MOS devices. This noise model tends to underestimate the channel noise of short-channel transistors [28]. The existing long-channel noise model has been adopted by most model developers through assigning a larger channel noise parameter γ that is no longer constant and changes with both bias and device dimensions to accommodate larger than expected noise of short-channel MOS transistors. While such a modification is convenient, it does not capture the noise of short-channel devices accurately, especially as the drain-source voltage or the lattice temperature of the device changes. Extraction of such empirical parameter γ to fit to all measured noise data is also very cumbersome.

In [21], the channel noise of ballistic NMOS transistors has been attributed to the shot noise induced by random injections of electrons from the source to the channel, whereas the thermal noise in the channel has been completely eliminated. The current noise spectral density of the channel has been described by $2qI$ following the shot noise model in vacuum tubes (which are ballistic devices). This simple model has been compared with device simulation data. To the authors' knowledge, no verification of this noise model with measured noise performance has been provided since.

The shot noise model is built upon the ballistic transport theory, in which the electrons, after tunneling into the channel, are pumped into the drain immediately without any scattering. Given the doping density in the channel of NMOS transistors in this technology, the electron mean free path is roughly 7 nm [29], leading to each electron encountering on average 6 scattering events in the channel ($L \approx 40$ nm). Adding the Si-SiO₂ interface scattering further increases the number of scattering events experienced by each electron. Therefore, for such semi-ballistic devices, noise contributions from both thermal and shot noise must be considered, as depicted in Fig. 4, leading to the effective channel noise spectral density $\overline{i_{Ch}^2}$ given by

$$\overline{i_{Ch}^2} = \overline{i_{sh}^2} \cdot \left(\frac{1 + g_m R_{DS}}{1 + g_m R_{DS} + g_D R_{DS}} \right)^2 + \overline{i_{th}^2} \cdot \left(\frac{g_D R_{DS}}{1 + g_m R_{DS} + g_D R_{DS}} \right)^2 \quad (3)$$

Fig. 4. (a) Equivalent noise circuit model of a MOSFET with various noise sources. (b) The inset depicts the noise mechanisms in the channel for short-channel MOSFETs. (c) Circuit representation of the two noise sources inside the intrinsic transistor transport region.

Fig. 5. Comparison of measured (open symbols) and simulated (solid lines) S-parameters under different gate-source voltage V_{gs} (0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V) and a fixed drain-source voltage $V_{ds} = 1.2$ V for an NMOS transistor with a width of 84 μm . The frequency spans from 2 to 40 GHz.

where R_{DS} is the output resistance, g_m is the device transconductance and g_D is the N/N+ junction diode (channel to source) forward bias conductance. This N/N+ junction diode at the virtual source is a non-ideal diode, leading to the introduction of a fitting noise parameter $\zeta = \frac{g_D R_{DS}}{1 + g_m R_{DS} + g_D R_{DS}}$ in the following equation.

$$\overline{i_{Ch}^2} = \overline{i_{sh}^2} \cdot (1 - \zeta)^2 + \overline{i_{th}^2} \cdot \zeta^2 \quad (4)$$

In the above equations, $\overline{i_{sh}^2}$ is the shot noise used to describe the noise associated with the tunneling of electrons at the source-channel barrier, and $\overline{i_{th}^2}$ is the thermal noise in the channel given by $\overline{i_{Ch}^2} = 4g_k T g_0$ with γ of 2/3 in saturation and 1 in linear region. The correlation between the two noise sources $\overline{i_{sh}^2}$ and $\overline{i_{th}^2}$ is ignored as the two noise mechanisms are spatially separated. The noise equivalent circuit model is depicted in the schematic shown in Fig. 4(a). Figs. 4 (b) and (c) depict the noise mechanism in the device. The combination of the shot and thermal noise models not only predicts the drain current noise accurately, but also captures the undying physics very well. The noise sources in Fig. 4 (a) consist of the thermal noise from three access resistors of the three terminals of the device, *i.e.* $\overline{i_D^2}$, $\overline{i_G^2}$, $\overline{i_S^2}$ and the combined shot-thermal noise from the channel, *i.e.* $\overline{i_{Ch}^2}$, given by (4). By matching to the measured noise data, it has been experimentally found that there is no need for accounting for the induced gate noise or distributed

gate resistance, at least for the transistor geometries (widths of 40 μm to 320 μm) and frequencies (2 - 40 GHz) measured in this work.

The high frequency noise characteristics of a two-port system can be represented by

$$NF = NF_{min} + \frac{4R_n}{Z_0} \frac{|\Gamma_{opt} - \Gamma_s|^2}{|1 + \Gamma_{opt}|^2 (1 - |\Gamma_s|^2)} \quad (5)$$

where NF is the noise factor (also termed as noise figure when reported in decibels) at a given source reflection coefficient Γ_s . NF_{min} is the minimum noise factor. Γ_{opt} is the source reflection coefficient for minimum noise factor and $Z_0 = 50 \Omega$ is the characteristic impedance of the system. R_n is the equivalent noise resistance, which is a measure of how fast the noise figure degrades as the source reflection coefficient deviates from its optimum value Γ_{opt} . An accurate NF prediction requires an accurate modeling of four noise parameters: NF_{min} , R_n , and complex Γ_{opt} . Fig. 5 depicts a comparison between the measured S-parameters and simulated S-parameters (using SpectreRF) based on this model for an 84 μm transistor under different V_{gs} (0 V, 0.3 V, 0.6 V, 0.9 V, 1.2 V) and a fixed $V_{ds} = 1.2$ V in the frequency range of 2 to 40 GHz. Note that an accurate high frequency equivalent circuit model is the premise to constructing this noise model with only one fitting parameter.

Fig. 6 shows the simulated noise parameters NF_{min} , R_n , and Γ_{opt} by three different models (the one developed in this work with the noise parameter $\zeta = 0.3$, the classical ideal

Fig. 6. Measured (open symbols) and simulated (lines) noise parameters with three different noise models: (a) NF_{min} and R_n as functions of frequency at bias $V_{gs} = 0.5$ V and $V_{ds} = 1$ V, (b) NF_{min} and R_n as functions of frequency at bias $V_{gs} = 1$ V and $V_{ds} = 1$ V, and (c) Γ_{OPT} plotted on a Smith impedance chart for an NMOS transistor with a width of 84 μm . The noise parameter $\zeta = 0.3$. Note that, the mismatch in NF_{min} at frequencies between 26 and 40 GHz is due to the measurement issues as it appears in all the noise data.

long-channel thermal noise model with γ of 2/3, and the post-layout foundry model with a bias and size dependent γ compared to the measured data. The foundry model and the classical model both underestimate the minimum noise figure by ~ 1 dB and ~ 0.5 dB, respectively. Moreover, the classical channel noise model and the foundry model predict that the equivalent noise resistance is almost flat within a broad range of frequencies, which is in contradiction with the measured data. Additionally, the foundry model and the classical model underestimate the equivalent noise resistance, which means that a small mismatch of the source impedance leads to a large discrepancy in the overall noise figure. Compared to the foundry model and the classical thermal model, the model developed in this work delivers a much more accurate prediction of all four noise parameters, leading to accurate noise figure predictions for all impedance values across the Smith chart. Note that in the frequency range between 26 to 40 GHz, an abrupt drop of NF_{min} is observed in the measurement data for all measured transistors (different sizes) and under different bias combinations. As the noise figure cannot decrease or fluctuate with increased frequency, the observed trend of NF_{min} between 26 to 40 GHz are most likely due to a measurement-related issue, which is still under investigation. Such measurement-related issues were much less severe for R_n , and Γ_{opt} measurements.

Fig. 7 depicts the extracted noise parameter ζ under different

Fig. 7. Extracted noise parameter ζ under different drain current values for 42 μm and 84 μm NMOS transistors.

Fig. 8. Comparison among drain current noise spectral densities calculated by different channel noise models as functions of drains-source voltage V_{ds} , whereas gate-source voltage V_{gs} is kept at 0.5 V for an NMOS transistor with a width of 42 μm .

biasing scenarios for transistors with two different sizes. As can be seen, this noise parameter ζ is roughly 0.3, independent of bias, geometry or frequency. In comparison, available models use at least two parameters (γ and noise correlation factor) that are both bias and geometry dependent.

With respect to the device operating region, classical thermal noise model predicts that the noise spectral density should decrease from linear region with $\gamma = 1$ to saturation region with $\gamma = 2/3$. This change is in direct contradiction with the observed trend of the extracted noise spectral density shown in Fig. 8. The extracted channel noise (red curve) follows the trend of the shot noise but has smaller values.

V. MODEL VALIDATION

In order to further verify the model accuracy, a two-stage microwave low noise amplifier (LNA) has been implemented in the same technology and the measured performance is compared with the simulation result based on this model.

The circuit schematic of the two-stage microwave LNA is depicted in Fig. 9 (a). The LNA consists of two common-source stages with a 126 μm wide transistor in the first stage and an 84 μm wide transistor in the second stage. The gain and noise figure at 50 Ω input impedance have been measured using a Keysight N8975A Noise Figure Analyzer with INFINITI GSG

Fig. 9. (a) The circuit schematic of a two-stage microwave LNA. The first stage uses a 126 μm wide transistor while the second stage has an 84 μm wide transistor. (b) The comparison between measured and simulated S_{21} and Noise Figure of the LNA (50 Ω source impedance) vs. frequency. Noise data was only available up to 26.5 GHz.

RF probes. The S-Parameters of the LNA are also measured using a Keysight E8361A PNA. Moreover, the circuit is simulated using SpectreRF with both the foundry-supported process design kit (PDK) and the transistor model developed in this work (MVS as core drain current model, parasitic elements calibrated with measured data) in combination with models of passive devices (inductors and capacitors) from the post-layout extraction. Fig. 9 (b) shows a comparison among the simulated and measured forward gain S_{21} and noise figure at 50 Ω input impedance of the LNA. A close agreement between the measured data and simulated data based on this model is observed for both gain (S_{21}) and noise figure from 10 to 30 GHz (Noise data are measured up to 26 GHz). The simulated circuit performance based on the foundry PDK underestimates both gain (by as much as 5 dB) and noise figure (by about 1.3 dB).

VI. CONCLUSION

A new combined shot-thermal channel noise model that predicts the high frequency noise behavior of NMOS transistors has been developed. Through the combination of shot noise and ideal long-channel thermal noise, the model developed in this work is capable of capturing the device physics and achieving an excellent noise prediction. It is found that induced gate noise model and distributed gate resistance model are not required to capture the noise behavior of these transistors. The developed noise model uses only one fitting parameter ζ , which is not geometry, bias or frequency dependent. The model overcomes the limitations of most existing thermal-noise based models which use bias, geometry

and sometimes frequency dependent parameters in predicting the noise of sub-100 nm channel length transistors.

The model accuracy is confirmed through comparison with measurement of a two-stage microwave LNA. The close agreement between the measured and simulated gain and noise parameters indicates that the model is ready for practical RF and microwave circuit design.

Effects such as gate oxide breakdown, drain-source reach-through, kink effect observed in PD-SOI transistors, gate distributed resistance, low-frequency noise, low-frequency dispersion of device transconductance and output resistance, device lifetime and statistical variations of device parameters have not been modeled in this work. While this work has focused on developing an accurate scalable large signal noise model for 45 nm NMOS SOI transistors, the proposed noise modeling may be applicable to other CMOS and CMOS-SOI devices.

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