An Ultra-Wideband CMOS PA with Dummy Filling for Reliability

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Abstract

A V-band power amplifier in a bulk 65 nm CMOS technology with a peak gain 14.5 dB and 3-dB bandwidth of 28.8 GHz (50.8 GHz to 79.6 GHz) is presented. The techniques to boost bandwidth and power efficiency are presented. In addition, the design of dummy filling to satisfy manufacturing density requirements while having negligible effects on performances is discussed in details. The PA features a three stage transformer coupled differential architecture with integrated input and output baluns on-chip. The PA achieves a measured saturated output power of 15.1 dBm and output 1 dB compression power of 12.9 dBm at 65 GHz. The peak power-added efficiency is 18.9 %. The entire PA occupies area of 0.31 mm², while consuming 150 mW from a 1.25 V supply.

Keywords: CMOS, power amplifier, transformer, V-band

1 Introduction

The unlicensed multi-gigahertz bandwidth around 60 GHz is a good candidate for high data rate, short-range, and point-to-point wireless communication systems. CMOS technologies are attractive for the advantages of low power consumption, low cost, and high level integration with baseband. A CMOS-based 60 GHz power amplifier remains a challenge mainly due to low output power and low power added efficiency (PAE). Power combining techniques are typically used to achieve higher output power, albeit at the cost of reduced efficiency. For the high speed and wide bandwidth data communication applications, the PA is required to broaden the operation bandwidth. The main challenge of designing a PA over a broadband frequency range is to simultaneously match the optimum load impedance and maintain broadband gain performance. Distributed amplifiers are well-known approaches for wideband application, but large power dissipation degrades power efficiency. Also, distributed amplifiers usually occupy large chip area. A large number of 60 GHz PAs have been reported [1-11] over the past decade. However, trade-offs are still challenging between key specifications, such as gain, power efficiency, and bandwidth. Therefore, techniques to boost power amplifier bandwidth while maintaining high output power and high efficiency are desired.

CMOS technologies' rapid advancements over the past decade support increasing circuit speed, resulting in the wide adoption of mm-wave CMOS circuits today. However, the CMOS mm-wave power amplifiers are still challenging. First, although intrinsic CMOS device speed keeps increasing, the shrinking power supply voltages challenge high power delivery. Second, lossy substrates and high contact resistance degrade the quality factor of

passive components and decrease power efficiency. Third, a larger portion of parasitic capacitance versus intrinsic capacitance erodes achievable operating frequency and further wastes power through the additional charging/discharging current to the parasitics. In addition, the main drive for CMOS technologies for integration with analog and digital sub-systems for SOC, on the other hand, imposes large coupling and interference among circuit blocks. Moreover, deep-scaled technologies have very tight design rule check (DRC) requirements, including local and global density requirements to ensure reliability. These requirements therefore impose a significant challenge to high frequency design with the need of passive components, such as inductors and transformers. To overcome these challenges in deep-scaled CMOS technologies, we adopted a transformer-based output matching network. The matching network transforms the 50 Ω output load impedance to the optimum load impedance over a broadband frequency to achieve high output power and PAE. The offset frequency tuning scheme and transformer based inter-stage matching network were used to obtain broadband gain performance. Moreover, well-designed metal dummy filling is presented to increase PA reliability.

This paper is organized as follows. Section 2 discusses the design details of the transformer coupled differential wideband PA to enhance the bandwidth and increase power efficiency. Section 3 presents the detailed theoretical analysis of dummy effects and provides design insight for dummy filling for high reliability while minimizing performance degradation. Section 4 presents measurement results, and is then followed by a conclusion in Section 5.

2 Wideband PA design

Fig. 1. Topology of the three-stage differential PA.

Fig.1 presents the schematic of a transformer-coupled three-stage differential PA with integrated input and output baluns. Transformer based inter-stage matching and tuning is adopted due to its advantages of compactness, differential configuration, and good isolation between input and output for better stability. Also, DC biasing is applied at the center tap of the transformer, so DC block capacitors, RF chokes, and bypass capacitors can be eliminated for a considerable space reduction. The input and output transformers serve as baluns to convert between single-ended I/O signals and differential on-chip signals. Each stage is a differential NMOS common-source amplifier to achieve larger headroom and higher linearity.

2.1 The Wideband Transformer-based Output Matching Network

To achieve high output power and high efficiency over the entire frequency range, the output matching network should be designed to transform the load to the optimum impedance across the entire frequency range of interest. The optimum impedance is determined by performing large-signal load-pull simulation and it can be represented as [12]:

$$Z_{opt} = R_{opt} \parallel X_{opt} \quad (1)$$

The parallel resistive portion R_{opt} is chosen for maximum peak PAE, and the device output capacitance C_{device} is tuned out by choosing

$$X_{opt} = -\frac{1}{j\omega C_{device}} \quad (2)$$

Fig. 2. Broadband optimum load impedance for a pair of differential pair transistor with the size of 89.44 μm/ 60 nm

A large signal, load-pull simulation for maximum peak PAE is performed for a differential common-source amplifier with a transistor width of 89.44 μm from 55 GHz to 75 GHz. As shown in Fig.2, the optimum impedance fits the Z_{opt} where $R_{opt} = 71.43 \Omega$ and $C_{device} = 58.77$ fF. To achieve a broadband operation PA, we employed a transformer based matching network to transform the 50 Ω output load to the optimum impedance across the operation frequency range.

Fig. 3. Equivalent circuit model of the transformer-based matching network.

Fig.3 shows the equivalent model of the output stage with a transformer based matching network [13]. The output device is modeled as a current source shunt with a parallel RC network. Here, C_{device} represents the drain capacitance of the transistor, and R_{opt} is determined through large signal load-pull simulation. The output matching network is composed of a transformer and a shunt capacitor C_2 , which comes from the output pad and the transformer parasitics. The transformer is modeled with two coupled inductors, L_1 and L_2 , with coupling coefficient k . Here, R_{s1} and R_{s2} represent the parasitic resistances of the inductors L_1 and L_2 , respectively. The mutual inductance M is:

$$M = k\sqrt{L_1 L_2} \quad (3)$$

To simplify the analysis, we make the self-resonant frequencies on the primary and secondary sides identical by setting:

$$\omega_0 = \frac{1}{\sqrt{L_1 C_{device}}} = \frac{1}{\sqrt{L_2 C_2}} \quad (4)$$

In addition, the inductance ratio is equal to the impedance transformation ratio of $L_2/L_1 = R_{load}/R_{opt}$. With the above requirements, the transfer impedance of the network is given by

$$\frac{v_o}{i_{in}} = sM / [k^2 \left(s \frac{L_1}{R_{opt}} + \frac{s^2}{\omega_0^2} \right)^2 - \left(1 + \frac{R_{s1}}{R_{opt}} + s \left(\frac{L_1}{R_{opt}} + C_1 R_{s1} \right) + \frac{s^2}{\omega_0^2} \right) \left(1 + \frac{R_{s2}}{R_{load}} + s \left(\frac{L_2}{R_{load}} + C_2 R_{s2} \right) + \frac{s^2}{\omega_0^2} \right)] \quad (5)$$

The transfer function of this network is comprised of two conjugate pole pairs. If the inductors are ideal components; $R_{s1} = R_{s2} = 0$; the two resonant frequencies can be simplified as

$$\omega_{L,H} = \omega_0 \sqrt{\frac{1}{1 \pm k}} \quad (6)$$

Fig. 4. Frequency response versus coupling coefficient of the transformer model at different coupling coefficient

Fig.4 presents the transfer impedance frequency responses with different coupling coefficients. In this simulation, Q-factors of 15 and 10 were assumed for the primary and secondary inductors, respectively. As shown in Fig.4, the inductor's parasitic resistance causes higher loss as frequency increases. Therefore, instead of making mid-band close to center frequency (65 GHz), ω_L is chosen close to the center frequency.

Fig.4 shows that higher coupling coefficient leads to higher gain. This is due to the fact that the equivalent inductance with higher coupling coefficient drops, as presented by combining Eqs.(4) and (6):

$$L_1 = \frac{1}{\omega_L^2 C_{device} (1+k)} \quad (7)$$

Smaller inductance introduces smaller parasitic resistance and causes less loss. Therefore, to minimize the insertion loss from 55 to 75 GHz, a coupling coefficient of > 0.7 is preferred.

Fig. 5. (a) The simulated trace width versus the coupling coefficient of the vertical-coupling transformer (b) The simulated trace space versus the coupling coefficient of the horizontal-coupling transformer.

There are two types of commonly used on-chip transformers. One is the vertical-coupling and the other is the horizontal-coupling type as shown in Fig.5(a) and (b), respectively. To maximize the Q-factors, the primary and

secondary windings are implemented using top two thick layers, which are 3.4 μm and 0.9 μm , respectively for the vertical-coupling structure, and the top layer is used for both windings in the horizontal-coupling structure. Fig.5 shows the simulated coupling coefficient of these two types of transformer at 65 GHz. In the simulation, all the primary winding inductances are fixed at 120 pH. It shows that even with the minimum space of 2 μm , the coupling coefficient of the horizontal-coupling structure is less than 0.6. Therefore, the vertical-coupling transformers are adopted in this design due to their large coupling coefficient.

The transformer width is chosen with the tradeoff consideration of quality factor Q and the self-resonant frequency. Fig.6 shows the simulated primary windings Q-factors at 65 GHz and the transformer self-resonant frequency versus trace width at the fixed primary inductance 120 pH. To decrease the loss from the matching network, high Q-factor transformers are required. Since the Q-factor doesn't increase appreciably with trace widths larger than 4 μm , to achieve a large self-resonant frequency, the trace width of 4 μm , which has $k = 0.76$ and $Q = 17$, is adopted for the transformer based output matching in this design. The output pad and the transformer parasitic capacitance contribute to C_2 in Fig.3. To reduce the loss caused by C_2 , there is no explicit shunt capacitor at the output.

Fig. 6. Simulated Q-factor and minimum insertion loss as a function of trace width of a vertical-coupling transformer

Fig.7 shows the simulated frequency response and the impedance of the designed transformer based matching network. The minimum insertion loss is 0.89 dB, and the 1-dB bandwidth is from 48 GHz to 84 GHz.

Fig. 7. (a) Insertion loss of the output matching network and (b) impedance of the ideal case (black) and the designed (blue) matching networks

2.2 Offset frequency tuning

To realize wide band performance of the PA, an offset tuning frequency scheme is adopted. Since the transistors' size increases from the first to last stage, their $G_{\max}$ and $f_{\max}$ values decrease toward the output side. Therefore, the resonant frequency of the first stage is designed to be higher than that of the second stage, which is in turn higher than the third stage resonant frequency.

In a multi-stage power amplifier, the power gain, output power, and efficiency of each stage have an impact on the overall PA performance. The last stage is designed to maximize the peak PAE and achieve a high level of output power over a wide frequency range, and the driving stages are optimized to achieve high efficiency and flat gain response over a wide frequency range.

The overall PAE of a three-stage is equal to:

$$PAE \approx \frac{1}{\frac{1}{PAE_3} + \frac{1}{G_3 PAE_2} + \frac{1}{G_2 G_3 PAE_1}} \quad (8)$$

where PAE_1, PAE_2 , and PAE_3 are the first, second, and last stage PAE, and G_1, G_2 , and G_3 are the first, second, and last stage power gain, respectively. Eq. (8) indicates that the last stage PAE is dominant and the first stage PAE has the least impact on the overall power efficiency. Therefore, the first stage tuning frequency is chosen to achieve broadband, flat power gain response. This offset tuning frequency scheme facilitates smooth wideband gain response as shown in Fig.8 and maintains high output power and high efficiency.

Fig. 8. Simulated power gain for each stage and the overall PA gain versus frequency

2.3 Transformer-based Inter-stage Matching Network

Transformer-based inter-stage matching is adopted because of its advantages of compactness and bias isolation. Different transformer matching scheme is chosen for each individual stage for different design goals.

As discussed in Section 2.1, the 1:1 transformer is used in the last stage to transfer R_{load} to R_{opt} based on the load pull requirements for high efficiency and high output power. As for the matching of internal stages, stages 1

and 2, a larger conductance transformation is needed due to the large mismatch between the conductance of the transistor's drain (X_d) and the conductance of the transistor's gate (X_g). A 2:1 transformer is adopted for the matching network between the second and third stage, since the large conductance transformation is accomplished by the primary inductance of two-turn inductor. Additionally, the Q-factor of 2:1 transformer is optimized to achieve high efficiency.

Fig. 9. Comparison inter-stage matching network using (a) 1:1 transformer with transmission line (b) 2:1 transformer from 40 to 90 GHz

Fig. 10. Comparison of two matching topologies in: (a) reflection coefficient at plane X in Fig. 9 (b) power gain for 1st stage and the overall PA gain

In order to further enhance the bandwidth, a different transformer matching scheme is chosen between the first and second stages. Instead of using 2:1 transformer, a 1:1 transformer with a transmission line is adopted. Fig.9 shows the half circuit model and Smith chart impedance transformation of the two matching topologies. In this simulation, Q-factors of 15 and 10 were assumed for the primary and secondary inductors, respectively and a coupling coefficient of 0.75 is assumed. For the 1:1 transformer, $L_p \approx L_s$; while, $L_p \approx 2L_s$ for the 2:1 transformer. With additional transmission lines, the primary inductance, L_p , can be reduced, and then reduce

the shunt magnetizing inductance, M in the equivalent model. As shown in Smith chart, both of the two matching topologies can achieve impedance matching at 80 GHz. But, the 1:1 transform which has smaller M facilitates susceptance transformation at lower frequencies. The reflection coefficients at plane X of the two matching topologies are shown in Fig.10(a). It shows that with 1:1 transformer with the transmission line, the good matching is achieved not only at 80 GHz but also at 50 GHz, and then further boosts the bandwidth as shown in Fig.10(b).

2.4 High efficiency active device design

Fig. 11. (a) Optimal PA transistor layout and (b) the layout of each unit

One of major challenges of the mm-wave PA design is the active device optimization. Since the nanoscale CMOS processes cannot handle high voltages, a high output power delivery requires a large transistor width (W). The use of large transistors in the PA increases device parasitics which constrain the power gain and efficiency. Therefore, it is critical to optimize the finger width (W_F) and the number of fingers (N_F) to minimize parasitics for the highest maximum stable gain (MSG) and drain efficiency. The unity power gain frequency ($f_{\max}$) can be approximated as

$$f_{\max} = \frac{f_T}{2\sqrt{R_g \left(g_m \frac{C_{gd}}{C_{gt}} \right) + (R_g + r_{ch} + R_s) g_{ds}}}; \quad f_T = \frac{g_m}{2\pi C_{gt}} \quad (9)$$

where f_T is the unity current gain frequency, g_m is the transistor's transconductance, C_{gt} is the gate total capacitance, g_{ds} is the transistor's output conductance, and R_g , r_{ch} and R_s are the gate, channel, and source resistances, respectively. From the equation, $f_{\max}$ is highly-dependent on the resistive losses, especially the value of R_g . The R_g of each individual finger is proportional to W_F/L where W_F is the finger width and L is the channel length. A large W_F results in a large gate resistance, which causes increased losses in the transistor, thereby reducing $f_{\max}$ and the MSG of the transistor. However, a smaller W_F leads to an increase of the N_F and the interconnect length, which introduces parasitic resistance and inductance to degenerate the transistor performance. Therefore, layout optimization becomes essential for high performance. To avoid long interconnects around the transistor, the large transistor is

Fig. 12. Load-pull simulated (a) peak PAE and (b) P_{sat} and $P_{1\text{dB}}$ versus the number of parallel transistor units

divided into several transistor units and connected in parallel as shown in Fig.11(a). Fig.11(b) shows the layout of the unit transistor cell used in this design. The source lines are distributed with wide metal tracks on both metal 1 and metal 2 to minimize the source impedance. Double gate connection is used to further reduce the serial gate resistance. In addition to reducing the length of the overall interconnects, the layout structure simplifies the input and output connection. As shown in Fig.12, the transistor layout with 4 PA units connected in parallel leads to an optimum layout and maximizes the transistor efficiency.

3 Dummy filling for reliability

In the chemical-mechanical polishing (CMP) process, the metal density dependent variation in the interlevel dielectric thickness reduces yield and impacts circuit performance. Deep-scaled processes require metal density in local chip areas to reduce metal thickness variations and planarize the dielectric layers in the CMP process [16]. Conventionally, to avoid the EM coupling effects, high frequency passive components are often exempted from the metal density requirements. However, this layout style may degrade chip reliability in the long term. Therefore, metal dummy filling is required to satisfy all the density requirements, both locally and globally. Dummy fills affect the performance of the passive components due to the resultant eddy current which is induced by magnetic coupling to the dummy fills. Eddy current in dummy fills increases the loss, and the dissipation power caused by eddy current increases as the frequency increases. Also, the magnetic coupling between the signal current and the eddy current decreases

the wire inductance. Although metal dummies can be generated automatically, it is important to develop a dummy filling method that meets the local metal density requirements while having minimum effects on passive components.

Assuming the magnetic field, B_0 , is uniform over the area of the metal fill piece, and a circular metal shape is used to approximate a square metal fill. The power dissipation caused by eddy current in a circular metal fill with diameter W can be represented as [14]

$$P_{\text{eddy}} = \int \frac{V^2}{R} = \omega^2 B_0^2 \frac{\pi h}{8\rho} \left(\frac{W}{2}\right)^4 \quad (10)$$

where ρ is the resistivity, and h is the height of the metal fill.

If a large metal piece is divided into N^2 small metal pieces with diameter W/N , the dissipation power become

$$P_{\text{eddy}} = N^2 \cdot \omega^2 B_0^2 \frac{\pi h}{8\rho} \left(\frac{W}{2N}\right)^4 = \frac{1}{N^2} \cdot \omega^2 B_0^2 \frac{\pi h}{8\rho} \left(\frac{W}{2}\right)^4 \quad (11)$$

Eq. (11) indicates that the dissipation power caused by eddy current is reduced significantly by using isolated small dummy fills.

An octagonal winding can be approximated as a circular loop. Using the Biot-Savart law, the vertical magnetic field in the plane of the loop with current, I , can be represented as

$$B = \frac{\mu_0 I R}{2\pi} \int_0^{2\pi} \frac{R - x \cos \phi}{(x^2 + R^2 - 2xR \cos \phi)^{3/2}} d\phi = I \cdot B'(R, x) \quad (12)$$

where μ_0 is vacuum permeability, R is the loop radius, and x is the distance from the loop center. The magnetic field of a circular loop with different radius is plotted in Fig.13. It shows that the area surrounding the winding ($x/R=1$) has the strongest magnetic field, thus inducing large eddy current when dummy fills are close to the winding. The magnetic field drops significantly when the distance x is larger than $1.5R$. Therefore, to minimize the eddy current effect, the placement of dummy fills should avoid a strong magnetic field region which is the distance within $1.5R$.

Fig. 13. Normalized Magnetic field around the winding versus different normalized distance x/R

The definition of Q-factor is

$$Q = 2\pi \frac{\text{peak energy stored}}{\text{energy dissipated in a cycle}} \quad (13)$$

For the inductor L with parasitic resistance R_L , the Q-factor is converted into:

$$Q = 2\pi \frac{\frac{1}{2} L I_m^2}{P_{\text{dmy}} + P_{R_L}} \quad (14)$$

where I_m is the magnitude of the current of winding current, P_{dmy} , and P_{R_L} are the dissipation power caused from the dummy filling metal and the inductor's parasitic resistance, respectively. From Eq. (10) and (12), the power dissipated caused by eddy current is

$$P_{\text{dmy}} = \sum \omega^2 (I \cdot B'(R, x))^2 \frac{\pi h}{8\rho} \left(\frac{w}{2}\right)^4 = (I_m \cos \omega t)^2 \sum \omega^2 B'^2(R, x) \frac{\pi h}{8\rho} \left(\frac{w}{2}\right)^4 \quad (15)$$

The total dissipation power is then:

$$P_{\text{dmy}} + P_{R_L} = \int_0^T (I_m \cos \omega t)^2 \sum \omega^2 B'^2(R, x) \frac{\pi h}{8\rho} \left(\frac{w}{2}\right)^4 dt + \int_0^T (I_m \cos \omega t)^2 R_L dt \quad (16)$$

$$P_{\text{dmy}} + P_{R_L} = I_m^2 (\omega^2 X_{\text{dmy}} + R_L) \pi / \omega$$

where

$$X_{\text{dmy}} = \sum B'^2(R, x) \frac{\pi h}{8\rho} \left(\frac{w}{2}\right)^4 \quad (17)$$

The Q-factor thus becomes

$$Q = \frac{L\omega}{\omega^2 X_{\text{dmy}} + R_L} \quad (18)$$

Eq. (18) indicates that a higher frequency or a larger dummy equivalent resistance (X_{dmy}) leads to a smaller Q and a larger loss.

Fig.14 shows an inductor with dummy filling. The design parameters are the distance between the transformer metal conductor, d , the width, w , and the space, s .

Fig. 14. Topology of an inductor with dummy filling

Fig.15 shows the relationship between the dummy width and the Q-factor at 70 GHz of both calculation and HFSS simulation results versus different dummy widths w . To maintain the same dummy density, the space s changes accordingly with the distance from transformer to dummy d constant at $12 \mu\text{m}$. Both results agree with each other and the Q-factor increases as the width w becomes smaller.

Fig. 15. Calculated and HFSS simulated Q-factor of a dummy filled inductor versus different dummy width

To minimize the impact of metal dummies and satisfy the local density of at least 10 % for each metal layer, the small metal pieces with $w = 2 \mu\text{m}$ are chosen. To maximize the d , we use $s = 0.5 \mu\text{m}$ which is the minimum space meeting the design rule. Therefore, the density of the dummy filling region is 64 %, and then the maximum d value is used to satisfy 10 % local density.

Fig. 16. HFSS simulated results with the comparison of the transformer without dummy filling in: (a) Q-factor, (b) inductance, and (c) coupling coefficient.

This dummy metal filling optimization method is then applied to the transformer. For the transformer, whose diameter is $62 \mu\text{m}$ with dummy fillings width $2 \mu\text{m}$ and space $0.5 \mu\text{m}$, the maximum d is $18 \mu\text{m}$ and the calculated $\omega^2 X_{\text{dmy}}$ is 0.14Ω at 65 GHz . Fig. 16(a) compares the Q-factors of the primary and secondary inductors in four cases: without dummy filling, with optimized dummy filling, with automatic dummy filling HFSS simulation results, and with optimized dummy filling calculated results based on Eq. (18). It shows that our dummy addition method causes a small drop of the Q-factor by about 2.7 % at 65 GHz comparing with automatic filling causing a 35 % drop, and our analysis method is validated by simulation results. Fig. 16 (b) and (c) present the simulated inductance and coupling coefficient for cases both with and without dummy. It shows that the optimized metal filling has negligible impact. Also, the well-designed metal dummy filling makes the capacitance increase negligible, so the self-resonant frequency remains at 133 GHz after the metal filling

4 Measurement Results

Fig.17 shows the chip microphotograph of the V-Band PA implemented on a 65 nm bulk CMOS process with the dimensions of $0.43 \text{ mm} \times 0.73 \text{ mm}$ including testing pads. Small signal measurements were carried out with an Agilent N5247A PNA-X network analyzer which can perform measurements up to 67 GHz . From 67 to 80 GHz , the S-parameter is measured through a PNA-X network analyzer with Agilent N5260-60004 waveguide T/R modules (frequency extenders).

The PA consumes 150 mW from a 1.25 V supply at DC. The last stage transistors are biased at 22.5 mA to maximize small signal gain. Fig. 18 shows the measured S-parameters from two setups, one is carried out with a PNA-X up to 67 GHz ; the other is measured through a PNA-X with frequency extenders from 67 to 80 GHz . The PA exhibits a peak gain of 14.5 dB at 60 GHz with a 1-dB bandwidth of 17.5 GHz from 53.5 to 71 GHz and a 3-dB bandwidth of 28.8 GHz from 50.8 to 79.6 GHz . The input return losses are better than 5 dB from 45 GHz to 80 GHz . Since transmitters' input signals are near full scale voltage swing from signal sources, the gain of 14.5 dB is sufficiently high to generate power for a variety of applications.

Fig. 17. Photograph of the V-band PA.

TABLE 1 Performance comparisons with SOAs in 65 nm bulk CMOS

Ref.	B.W. [GHz]	OP1dB [dBm]	P _{sat} [dBm]	Peak Gain [dB]	Peak PAE [%]	Supply Voltage [V]	P _{dc} [mW]	Size [mm ²]
[1]	50-62	12.2	13.8	13.4	7.6	1.2	246	1.28
[2]	56.5-65	5	11.5	16	15.2	1	50	0.696
[3]	55-67	N/A	9.6	18.2	13.6	1.2	62.4	0.319
[4]	54-63*	10	14.6	23.2	16.3	1.2	135	0.6
[5]	57-66	9.3	12.9	16.7	23.4	1.2	61.2	0.11**
[6]	49-58	8.5	12.3	17.1	20.4	1	N/A	0.036**
[7]	55.5 - 62.5	13.7	14.85	9.4	16.2	1	N/A	0.357
[8]	N/A	N/A	9.6	29	17.3	1.2	N/A	0.1**
[9]	54-66	15.5	16.6	17.7	14.5	1.2	378	0.32**
[10]	48-74	9.5	13	13	6	2	N/A	0.048**
[11]	53-84	7.2	10.8	30.6	9.7	1.2	123	0.355
This work	50.8-79.6	12.9	15.1	14.5	18.9	1.25	150	0.31

* estimated from the presented figures, ** the size without the pads.

Fig. 18. Measured S-parameters results

For large signal characterization, a mm-wave signal generator was used to drive the PA into compression and the output power was measured with a power meter. The loss of probes, adaptors and cables were all de-embedded.

Fig. 19 shows the measured output power, power gain, and PAE as a function of input power at 65 GHz. The PA achieves a saturated output power (P_{sat}) of 15.1 dBm at 65 GHz with a power supply voltage of 1.25 V. The output 1 dB compression point (OP1dB) is 12.9 dBm and the peak PAE is 18.9 %.

Fig. 19. Measured output power, power gain and PAE versus input power at 65GHz.

Fig.20 shows the broadband characteristics of this PA. The measured OP1dB and P_{sat} with their PAE at 1.25 V bias from 55 GHz to 69 GHz in steps of 2 GHz are plotted in Fig.20.

Within the frequency range from 57 GHz to 69 GHz, the OP1dB is 11.7 ± 0.6 dBm with PAE from 10% to 12.8%, and the measured P_{sat} is 14.7 ± 0.5 dBm. The measured peak PAE is greater than 14% over 57 to 69 GHz. Both high output power performance and high efficiency are obtained from 57 GHz to 69 GHz, suggesting that the PA achieves an ultra-wide operation frequency range.

Table 1 summarizes the recently reported V-band PAs units in 65 nm bulk CMOS processes [1-11].

Fig. 20. Measured P_{out} , peak PAE, and PAE at $P_{1\text{dB}}$ as a function of frequency.

5 Conclusion

This paper presents a broadband three stage differential V-band power amplifier in a bulk 65 nm CMOS process. From 1.25 V supply, 14.5 dB small signal gain is achieved with saturated output power of 15.1 dBm and PAE of 18.9 % at 65 GHz. The PA demonstrates a bandwidth of 28.8 GHz in the 60 GHz band without capacitor tuning. From 57 GHz to 69 GHz, the peak PAE is greater than 14% and the saturation output power is 14.7 ± 0.5 dBm.

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7 References

- [1] T. Quemerais, L. Moquillon, S. Pruvost, J.-M. Fournier, P. Benech, and N. Carrao, "A CMOS class-A 65 nm power amplifier for 60 GHz applications," in *Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*, Jan. 2010, pp. 120–123.
- [2] W. Chan and J. Long, "A 58 GHz–65 Hz neutralized CMOS power amplifier with PAE above 10% at 1-V supply," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 554–564, 2010.
- [3] T. Wang, T. Mitomo, N. Ono, and O. Watanabe, "A 55–67GHz Power Amplifier with 13.6% PAE in 65 nm standard CMOS," *IEEE RFIC Symp.*, pp. 1–4, June 2011.
- [4] H. Asada, K. Matsushita, K. Bunsen, K. Okada, A. Matsuzawa, "A 60GHz CMOS power amplifier using capacitive cross-coupling neutralization with 16 % PAE", *EuMIC*, Manchester, pp. 1115–1118, Oct. 2011.
- [5] W.-H. Lin, T.-W. Huang, H. Wang, and J. Wang, "A 57–66 GHz 12.9-dBm Miniature Power Amplifier with 23.4% PAE in 65-nm CMOS," *EuMIC*, Amsterdam, pp. 12–15, Oct. 2012.
- [6] X. Bi, Y. Guo, J. Brinkhoff, L. Jia, L. Wang, Y. Xiong, M. S. Leong, and F. Lin, "A 60-GHz 1-V supply band-tunable power amplifier in 65-nm CMOS," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 58, no. 11, pp. 719–723, Nov. 2011.
- [7] J. Y.-C. Liu, R. Berenguer, and M. F. Chang, "Millimeter-wave self-healing power amplifier with adaptive amplitude and phase linearization in 65-nm CMOS," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1342–1352, May 2012.
- [8] J. Lin, C.C Boon, X. Yi, W. M. Lim, "A Compact Single Stage V-Band CMOS Injection-Locked Power Amplifier With 17.3% Efficiency," *IEEE Microwave and Wireless Components Letters*, col. 24, no. 3, pp. 182–184, 2014.
- [9] P. M. Farahabadi, and K. Moez, "A dual-mode highly efficient 60 GHz power amplifier in 65 nm CMOS," *IEEE RFIC Symp.*, pp. 155 – 158, Jun. 2014.
- [10] A. Larie, E. Kerhervé, B. Martineau and D. Belot, "A wideband 65nm CMOS transformer-coupled power amplifier for WiGig applications," *IEEE EuMIC*, pp. 41–44, Oct. 2014.
- [11] Po-Han Chiang, Wei-Heng Lin, Tzu-Yuan Huang, Huei Wang, "A 53 to 84 GHz CMOS power amplifier with 10.8-dBm output power and 31 GHz 3-dB bandwidth," *IEEE International Microwave Symposium*, pp. 1–3, Jun. 2014.
- [12] H. Wang, C. Sideris, and A. Hajimiri, "A CMOS broadband power amplifier with a transformer-based high-order output matching network," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2709–2722, Dec. 2010.
- [13] P. C. Huang, Z. M. Tsai, K. Y. Lin, and H. Wang, "A 17–35 GHz broadband, high efficiency PHEMT power amplifier using synthesized transformer matching technique," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 1, pp. 112–119, Dec. 2012.
- [14] F. Zhang and P. Kinget, "Design of components and circuits underneath integrated inductors," *JSSC*, pp. 2265–2271, 2006.
- [15] Y.-T. Chang, Y. Ye, C. Domier and Q. J. Gu, "A ultra-wideband CMOS PA with dummy filling for reliability," *Wireless Symposium (IWS)*, 2015 IEEE International, Shenzhen, 2015, pp. 1–4.
- [16] B. E. Stine, D. S. Boning, J. E. Chung, L. Camilletti, F. Kruppa, E. R. Equi, W. Loh, S. Prasad, M. Muthurishnan, D. Towery, M. Berman, and A. Kappor., "The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing processes," in *IEEE Transactions on Electron Devices*, vol. 45, no. 3, pp. 665–679, Mar 1998.