1 A 72% Error Reduction Scheme Based on Temperature Acceleration for Long-Term
2 Data Storage Applications: Cold Flash and Millennium Memories
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1 **Abstract**

2 A solid-state drive (SSD) with 1Xnm triple-level cell (TLC) NAND flash is proposed
3 for low cost data storage applications with long-term data-retention requirements.
4 Specifically, cold data storage requires 20 years data-retention with 100 write/erase
5 (W/E) cycles, whereas digital archive storage requires 1000 years retention time with 1
6 W/E cycle. To achieve these requirements, a flexible- n LC scheme is proposed to
7 improve the reliability of 1Xnm TLC NAND flash [1]. The proposed scheme combines
8 two schemes, n -out-of-8 level cell (n LC) [2] and asymmetric coding (AC) [3] with the
9 addition of a vertical flag. By measuring 1Xnm TLC NAND flash memory, the
10 proposed scheme reduces errors by 72% and 69% for digital archive and cold flash
11 respectively, compared to the conventional n LC scheme.

12
13 **Keywords:** solid-state drive, SSD, NAND flash memory, data archive, cold flash
14

1. Introduction

The solid-state drive (SSD) has the advantages of fast write and read speeds and high reliability compared with other types of data storage such as the hard disk drive and optical disk drive. SSDs are also highly reliable because, unlike hard disk and optical drives, they do not include mechanical components, which might malfunction due to physical wear and tear. Therefore, SSDs are well-suited to store cold data and archive data on enterprise servers, which need 20 and 1000 years retention time, respectively [1]. In this work, 1Xnm TLC NAND flash is used to achieve the lowest cost storage system, due to its capacity to store 3 bits in one memory cell [4]. However, the reliability of 1Xnm TLC NAND flash is lower compared with previous NAND flash generations that have larger cell size, or store fewer bits per cell [5]. In the small cell size of the 1Xnm generation, the number of electrons stored in the floating gate is significantly lower, which negatively impacts data-retention time [6]. In addition, because there are 8 possible threshold voltage (V_{TH}) levels in the TLC NAND flash cell, the voltage margins between V_{TH} levels are narrower than in the multi-level cell (MLC) and single-level cell (SLC) NAND flash, which have 4 and 2 V_{TH} levels, respectively. The reduced V_{TH} margins in 1Xnm NAND flash causes higher bit-error rates (BERs), which requires higher error correction ability to recover the errors, and also effectively degrades the data-retention time. Thus, the reliability of the 1Xnm TLC NAND flash SSD needs to be improved to simultaneously realize low cost and long-term data storage for 20 to 1000 years.

In NAND flash memory, reliability errors are mainly caused by program-disturb (PD), read-disturb (RD) and data-retention (DR), as described in Fig. 1. PD error and RD error are caused by an increase in V_{TH} due to the unwanted electron injection into the floating gate (FG) during program and read respectively [7]. On the other hand, DR error is caused by electron ejection from the FG and leads to decrease in V_{TH} [8].

During program, 2 types of voltage conditions can induce electron injection. First, in pass-through voltage (V_{pass}) disturb, all the unselected cells in the selected bit line experience a gate-source voltage of around 10V. The second V_{pgm} type of disturb occurs in the inhibited cells in the selected word line (WL) due to the potential difference between V_{pgm} (18V) and program inhibit BL voltage (8V).

Similarly, when NAND cells are read, read V_{pass} is applied to all the unselected WL's in the NAND block. Compared to PD, RD is a weaker effect because the read V_{pass} voltage is lower.

Fig. 1(a) shows measured bit-error rates (BERs) from a 1Xnm TLC NAND flash memory array. Bit error rate is calculated based on errors that occur in a single NAND

1 block, which is 2 MBytes. As data-retention time increases, DR errors also increase and
2 can become more than 100 times higher than PD errors [3]. In long-term storage, the
3 data is not frequently read [9]. Even when read frequency is 100 times per a day, there is
4 little difference in BER compared with BER without read disturb. Therefore, in
5 long-term storage, RD error is negligibly small. Thus, reducing the DR errors is key to
6 improve NAND flash reliability and obtain long-term data-retention.

7 Conventionally, schemes n -out-of-8 level cell (n LC) and asymmetric coding (AC) are
8 applied to 2Xnm TLC NAND flash and MLC NAND flash respectively to reduce DR
9 errors. In scheme n LC, “ n ” is the number of cell program levels, which is less than the
10 maximum number of levels, 8. By decreasing the number of possible V_{TH} levels stored
11 on the TLC NAND flash cell, significant BER reduction is obtained. For example, in
12 2Xnm TLC NAND flash, 10 years data-retention is achieved with 7LC at 85°C [2].
13 Note that 7LC achieves the lower cost than TLC (8LC) because TLC requires a stronger
14 by error-correcting code (ECC) and increases the cell area overhead of parity bit [2]. In
15 addition, DR error can be reduced by using the AC scheme, which re-arranges the data
16 to avoid high populations of data in the V_{TH} levels that have high error rates [3].

17 Fig. 2 shows the required data-retention time and write/erase (W/E) cycles for
18 different applications. Consumer SSD requires moderate endurance, e.g. 3000 W/E
19 cycles and moderate data-retention time, e.g. 3 years. Cold flash is used in
20 social-networking services to store photos and movies, which require infrequent
21 data-programming [10]. Therefore, lower 100-cycles endurance and longer 20-year
22 data-retention are needed. Lastly, the digital archive millennium memory requires only
23 one-time write and extremely long > 1000 years retention to preserve human digital data
24 such as culture, history and science information [11, [12]. Because the 1Xnm TLC
25 NAND flash has higher BERs than 2Xnm TLC NAND flash [13], the conventional n LC
26 scheme is not sufficient to meet the requirement of long-term data storage. In this work,
27 the reliability of 1Xnm TLC NAND flash is largely improved with the proposal, called
28 flexible- n LC. This scheme combines the conventional schemes n LC and AC by
29 proposing an additional vertical flag. Fig. 3 illustrates the architecture of the proposed
30 SSD controller by using the proposed scheme flexible- n LC. Our proposed controller
31 adds a “Program data encoder”, a “Data flip encoder”, a “Data to n -base coder” and
32 combines n LC and AC units, compared with conventional SSD controller [2].
33 Depending on the required data-retention time, “ n selector” and “AC selector” chooses
34 the optimum “ n ” and “1/0”s respectively. Flexible- n LC should always work with ECC
35 to reduce the effective BER to below recoverable BER levels. But the ECC encoder and
36 decoder are placed closer to the NAND flash than flexible- n LC since flex- n LC can also

1 increase the bit-errors by the decoding if the ECC does not first correct the bit-errors
2 during read [14]. Therefore, it can co-exist with any ECC such as advanced
3 soft-information ECC [16].

4 Whereas the previous work in [1] describes coding scheme optimization based on the
5 data-retention time only, this paper also investigates the optimal coding scheme when
6 1Xnm TLC NAND flash's W/E cycles, data-retention time and temperature are changed.
7 Furthermore, from these results, we confirm the effectiveness of the high temperature
8 acceleration test [17] to extrapolate the data-retention lifetime of the NAND flash
9 memory. Additionally, the activation energy (E_a) with different W/E cycles and ECC is
10 also investigated.

11 The paper is organized as follows, the reliability characteristics of 1Xnm TLC NAND
12 flash are measured and compared with 2Xnm TLC NAND flash in Section 2. In
13 Section 3, two schemes which improve the reliability of NAND flash, n LC and AC are
14 explained. Section 4 shows the improvement of data-retention time by using the
15 proposal flexible- n LC on the two types of long-term storage applications. Section 5
16 concludes this paper.

17 2. Reliability measurements of 1Xnm and 2Xnm TLC NAND flash

18 Fig. 4(a) shows measured BER during data-retention of 1Xnm TLC NAND flash at
19 room temperature (RT), 60°C, 85°C and 110°C, respectively. Only one W/E cycle is
20 applied to the memory array. The BER and retention time generally follows a linear
21 relationship in the log-log scale figure. Because of the limitation of measurement time,
22 the BER over one year data-retention time is extrapolated according to the formula [2],
23

$$24 \quad p = \alpha t^\beta \quad (1)$$

25 where, p is the projected BER and t is the data-retention time. The variables α and β
26 are different for each retention condition. Eq. (1) can be derived mathematically. After
27 100 years retention, the BER increases more than 10 times when retention temperature
28 is increased from RT to 85°C. Fig. 4(b) shows a previous work's measured BER during
29 data-retention on 2Xnm TLC NAND flash [2]. When this array is re-tested ("new data"
30 point on Fig. 4(b)), the new data matches the projected BER. This result confirms the
31 appropriateness of Formula (1) for the following analysis for long-term retention.

32 The maximum recoverable BER is limited by ECC [18-21] correction capability.
33 NAND flash array BER increases when data-retention time is increased and more W/E
34 cycles are applied [22]. As a result, the maximum data-retention time should be reduced
35 when the number of W/E cycles is increased, as shown in Fig. 5. In 1Xnm TLC NAND
36 flash, when the W/E cycle is one, the data-retention time is less than 10 years if the

1 temperature is higher than 85°C. Moreover, the data-retention lifetime is further reduced
2 when the W/E cycle increases. These retention times are insufficient to meet the
3 requirements of cold flash.

4 To understand the errors in detail, Figs. 6 and 7 show measured BER based on V_{TH}
5 levels, P1 to P7, during data-retention. Specifically, Figs. 6(a) [2] and 6(b) show
6 measured results of 2Xnm and 1Xnm TLC NAND flash, respectively, when the W/E
7 cycle is one. In both figures, V_{TH} level P7 has the highest BER when retention time is
8 long. In addition, the measured BER in 1Xnm TLC NAND flash shows more variation
9 than 2Xnm TLC NAND flash. The V_{TH} level P7 has higher initial BER and higher BER
10 variation, and the occurrence of errors is not evenly distributed in all 7 V_{TH} levels.
11 About 99% of the errors are caused by V_{TH} to its next lower level. As a result, the
12 dominant error is caused by V_{TH} shift from P7 to P6.

13 Figs. 7(a) and 7(b) show measured BER on 1Xnm TLC NAND flash after 100 and
14 200 W/E cycles. In less than one year, the BERs increase to >1%, which is the
15 maximum recoverable BER by using practical ECC schemes, such as
16 low-density-parity-check (LDPC) [23, [24]. Thus, to provide retention of 20 or 1000
17 years, additional techniques are needed to enhance 1Xnm TLC NAND flash's
18 reliability.

20 3. Conventional Schemes of n LC and Asymmetric Coding

22 3.1 Conventional scheme n LC

23 In a prior work, the n LC technique is proposed to reduce the DR error on 2Xnm TLC
24 NAND flash and increase the data-retention time [2]. Fig. 8 shows the concept of the
25 conventional n LC scheme [2]. Based on the measurements in Figs. 6 and 7, large BER
26 variation can be found depending on the V_{TH} levels, and thus, it is most efficient to
27 reduce the highest BER. Because most errors are caused when the V_{TH} decreases to its
28 next lower V_{TH} level, the scheme n LC removes the next lower V_{TH} level and adjusts the
29 read-reference voltages (V_{Ref}) to create a larger margin between V_{TH} levels. For example,
30 if P6 state is eliminated, V_{Ref7} should be removed to extend the P7's margin
31 (Fig. 8 (7LC)). Similarly, if P4 and P6 state are eliminated, V_{Ref5} and V_{Ref7} are also
32 removed (Fig. 8 (6LC)). The " n " represents the number of V_{TH} levels that are used for
33 storage. For instance, 7LC means 7 V_{TH} levels are used and one level is removed from
34 conventional 8 V_{TH} levels. To define the position of removed V_{TH} level, the terminology
35 "Mode-x" is used, as shown in Fig. 9. For instance, 7LC Mode-2 means 7 V_{TH} levels are
36 written in total, and the second V_{TH} level is the eliminated level. In n LC, the conversion

of binary data to n levels is conducted in the SSD controller.

3.2 Conventional scheme asymmetric coding

The concept of scheme AC is shown in Fig. 10. Because the 8 V_{TH} levels in TLC NAND flash have different BERs, as shown in Figs. 6 and 7, the reliability of TLC NAND flash can be improved by decreasing the occurrence of data in the V_{TH} level with high BER. The scheme AC is proposed to reduce the data population of the given V_{TH} level by selectively flipping the program data [3]. (Reducing the population of 1/0, in other words, means increasing the population of 0/1) In Fig. 10, the terminology “AC- x ” shows the number of V_{TH} levels that the data population was increased. For instance, AC-2 means that the data population on the second V_{TH} level is increased.

4. Proposed Flexible n LC Scheme

4.1 Introduction of flexible n LC

Figure 11 shows the distribution of NAND flash cell V_{TH} 's by using the proposed flexible- n LC (flex- n LC) scheme. Specifically, TLC NAND flash reliability is improved by combining n LC and AC. Figure 12 shows an example of program data transfer by using the proposed scheme with Mode-7 and AC-8, which eliminates 7th V_{TH} level (000) and increases the population of 8th V_{TH} level (010), respectively. In conventional TLC NAND flash, 8 V_{TH} levels are used to store 3 bits in each TLC NAND flash cell. However, in proposed scheme flex- n LC, the 7LC scheme stores only 7 levels, therefore data translation is needed. Fourteen-bit binary data from the host is first translated to 5 digits of base₇ data and the 7th V_{TH} level is eliminated [2]. Then, asymmetric coding increases the population of the 8th level (010) by bit flipping the 1st and 3rd pages. However, bit flip can have an undesirable effect of creating unwanted 7th level data. Therefore, the new vertical-flag area marks wherever the 7th level occurs, and data in that column is also flipped. Because the vertical-flag data is relatively sparse, compression is effective to reduce the overhead area, e.g., run-length encoding [25] and gzip [26] may shrink the vertical flag data area by 20% or 33%, respectively. The calculation and compression of vertical-flag data can also be handled in the SSD controller. Through the above process, fig. 13's (flex-7LC: Mode-7 + AC-8) V_{TH} distribution is obtained. Note that the flex- n LC decoder is very simple because the decoding only flips the data depending on the flag. Due to the simple logic, the latency, read performance degradation and circuit area related with the flex- n LC are negligibly small [3].

4.2 Improvement of NAND flash reliability

Fig. 14 shows measured NAND flash BER when 7LC is applied. All 8 possible modes are calculated, from Mode-1 to Mode-8. Each Mode removes one of the V_{TH} levels, as shown in Fig. 9. Mode-7 obtains the lowest BER by removing V_{TH} level P6, which is an expected result because P7 V_{TH} level has the highest BER, as shown in Figs. 6 and 7, and most errors are caused by V_{TH} decrease from P7 to P6. By removing the P6 state, a larger V_{TH} margin below P7 can be created to reduce the number of errors in the most unreliable memory state ('P7'). Furthermore, Fig. 15 shows measured NAND flash array BER by adding the asymmetric coding scheme together with the Mode-7. The options, AC-1 to AC-8, increase the NAND flash cell populations on each of the respective 8 V_{TH} levels. In Fig. 15, the proposed scheme of Mode-7 + AC-7 provides the minimum BER until 173 years retention. However, after 173 years, the optimum scheme switches to Mode-7 + AC-8. Therefore, to obtain the minimize BER, the coding scheme of flexible- n LC should be analyzed by considering the required data-retention time. Fig. 16 shows estimated BERs after 1, 10, 100 and 1000 years data-retention, respectively. The W/E cycle is 1 in these measurements. First, it is observed that the conventional TLC scheme has the highest BER, and BER can be reduced by applying the conventional 7LC scheme. However, the BER is still too high to be recovered by LDPC ECC, after 85°C 1000 years data-retention. To further reduce BER for 1000 years data-retention, the proposed flex- n LC schemes are applied. Specifically, by using the flex-7LC scheme, the measured BER is reduced by 72% compared with the conventional 7LC, and the BER is lower than 1% which can be recovered by ECC. In addition, greater BER reduction can be obtained by further reducing the number of V_{TH} levels to less than 7, however at the same time, cost is increased by decreasing the number of V_{TH} levels (n) due to capacity of data storage is reduced. Tanakamaru, *et al*, in [2] investigate the cost effective levels from the number of V_{TH} levels and the parity overhead of ECC. Although stronger ECC would increase the data-retention time, however, parity overhead would also increase which would decrease the cost effectiveness. The cost optimum V_{TH} level differs with required data-retention time [2]. As a result, overhead of the n LC due to the reduction of available V_{TH} level is minimized if we select the optimum coding with required data-retention time. Fig. 17(a) shows measured BERs when the W/E cycles are increased to 100. Because of array wear-out, the BERs in Fig. 17(a) is higher than in Fig. 14 which has only one W/E cycle. As a result, the number of V_{TH} levels needs to be decreased even further. The flex-6LC scheme is then applied to reduce the BER to less than 1% after 85°C 20 years data-retention. The proposed flexible-6LC scheme also

reduces BER by 69% compared with the conventional 6LC scheme. In Fig. 17(b), when the W/E cycles are increased to 200 cycles, 5 V_{TH} levels should be used. The proposed flexible-5LC successfully reduces the BER to less than 1% after 85°C 20 years data-retention. The proposed scheme flexible-5LC reduces BER by 60%, compared with the conventional 5LC. Note that V_{Ref} 's are fixed to be the same for all different measurements since the BER strongly depends on the V_{Ref} during read. Furthermore, there is the potential to enhance the reliability of NAND flash by combining with read retry [29] which improves the data-retention, which is kept as a future work.

In this paper, all the results are based on measurement of one NAND flash block. However, TLC NAND's BER can have a high variability between NAND flash blocks, chips, and vendors. Therefore, further study of variability is recommended.

4.3 Temperature acceleration of NAND flash memory

From Fig. 15 to Fig. 17, the optimum coding scheme changes depends on the number of NAND flash W/E cycles and data-retention time. Table I summarizes the optimum coding scheme depending on the 1Xnm TLC NAND flash W/E cycles, data-retention time and temperature. The optimum coding scheme which minimizes BER is selected depending on the W/E cycles, data-retention time, and temperature which application requires. Note that it must be selected before writing to the NAND flash since the coding cannot change during run-time. Further investigation is needed as a future work, since the optimum coding is likely to change depending on NAND flash generations and vendors. Because high temperature can accelerate the errors [30], the optimum coding scheme at RT may be suitable for shorter retention times at 85°C. As proof of this assumption, Table II shows that the optimum coding schemes at 85°C when data-retention time is 0.001-10 years, is similar to the optimum coding schemes at RT, with longer data-retention times, as shown in Table I. As a result, the equivalent data-retention time can be calculated from eq. (1) at RT and 85°C, by considering the similarity of optimum coding schemes. Fig. 18 shows equivalent data-retention times on RT and 85°C. Specifically, on 2Xnm TLC NAND flash, the BER after 1-year data-retention at 85°C is nearly equal to 50-year data-retention at RT, resulting in 50 times acceleration. On the other hand, the retention time acceleration increases to 600 times on 1Xnm TLC NAND flash, possibly because cell size scaling causes reliability degradation [6].

Generally, the Arrhenius equation has been used to estimate lifetime of semiconductor devices by temperature acceleration test, expressed as

$$L = A \cdot \exp\left(\frac{-E_a}{kT}\right) \quad (2)$$

where E_a is the activation energy, k is the Boltzmann constant, and T is the absolute temperature. Fig. 19 shows the Arrhenius plot of the data-retention lifetime with different W/E cycles with (a) LDPC ECC and (b) BCH ECC. As mentioned above, lifetime is defined when the BER reaches 1% and 0.1%, which are the limitations of recoverable BERs of LDPC and BCH ECC, respectively. It can be seen that E_a does not depend on ECC, however, with respect to W/E cycle, there is a large difference between W/E = 1 and W/E = 100, 200. Lower E_a has lower temperature dependency. Thus, high stressed NAND flash has reduced dependence on temperature. Highly stressed NAND flash has a higher initial BER than low stressed NAND flash. As a result, we suppose that the increasing rate of the BER is small. However, more investigation is needed about E_a with respect to different W/E cycles, its generation and the applied ECC, as a future research topic.

5. Conclusion

The scheme flexible- n LC is proposed for long-term storage applications such as archive and cold flash. Table III summarizes the results of this work. Compared to conventional n LC, the proposed flexible- n LC improves BER by 72% for archive and 69% for cold flash. Thus, with the flexible- n LC technique, the lowest-cost 1Xnm TLC NAND flash memory is also suitable, as is, for the long-term storage market. Furthermore, a precise match during retention of the optimum coding schemes at RT and 85°C are measured, which confirms that high temperature measurement is appropriate to accelerate room temperature testing.

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Fig. 1

Fig. 2

Fig. 3

Fig. 4

Fig. 5

Fig. 6

Fig.7

Conventional work

***n*-out-of-8 level cell (*n*LC) [2]**

8LC (TLC)

7LC (*n*LC)

6LC (*n*LC)

(i) Reduce the number of memory states.

(ii) Choose V_{ref} .

Fig. 8

Fig. 9

Fig. 10

Proposed work

Flexible- n LC (Flex- n LC)

flex-7LC

flex-6LC

The n LC distribution is written asymmetrically.

Fig. 11

Fig. 12

Fig. 13

Fig. 14

Fig. 15

Fig. 16

Fig. 17

Fig. 18

Fig. 19

List of table captions:

Table I: Summary of optimum coding scheme of flex-7LC at different write/erase cycles, data retention and temperature.

Table II: Summary of optimum coding scheme on short data-retention @85°C.

Table III: Summary of flex- n LC improvement.

		85°C				RT			
DR time (Year)		1	10	100	1000	1	10	100	1000
Write/erase cycle	1	Mode-7 + AC-7			Mode-7 + AC-8	Mode-7 + AC-4		Mode-7 + AC7	
	100	Mode-7 + AC-2				Mode-6 + AC-6	Mode-7 + AC-2		
	200								

Table I

		85°C				
DR time (Year)		0.001	0.01	0.1	1	10
Write/erase cycle	1	Mode-7 + AC-4			Mode-7 + AC-7	
	100	Mode-6 + AC-6	Mode-7 + AC-7	Mode-7 + AC-2		
	200	Mode-6 + AC-6				

The optimum coding is accelerated from RT.

Table II

Proposed	Applications	Bit error rate
Flexible <i>n</i> LC	<u>Archive: millenium memory</u> (W/E = 1, DR = 1k years)	-72% (Fig. 15)
	Cold flash (W/E = 100, DR = 20 years)	-69% (Fig. 16 (a))

Table III