Advanced Error-Prediction LDPC with temperature compensation for Highly Reliable SSDs

Authors: Tsukasa Tokutomi, Shuhei Tanakamaru, Tomoko Ogura Iwasaki, Ken Takeuchi

Organization:

Department of Electrical, Electronic, and Communication Engineering, Graduate School of Science and Engineering, Chuo University, 1-13-27 Kasuga, Bunkyo, Tokyo 112-8551, Japan

Return address:

Tsukasa Tokutomi

Chuo University

Department of Electrical, Electronic, and Communication Engineering, Graduate School of Science and Engineering

Chuo University Korakuen Campus Bldg. 2, 1-13-27 Kasuga, Bunkyo-ku, Tokyo 112-8551 Japan

PHONE: + 81-3-3817-7374

E-mail: tokutomi@takeuchi-lab.org

Abstract

To improve the reliability of NAND Flash memory based solid-state drives (SSDs), error-prediction LDPC (EP-LDPC) has been proposed for multi-level-cell (MLC) NAND Flash memory [1-2], which is effective for long retention times. However, EP-LDPC is not as effective for triple-level cell (TLC) NAND Flash memory, because TLC NAND Flash has higher error rates and is more sensitive to program-disturb error. Therefore, advanced error-prediction LDPC (AEP-LDPC) has been proposed for TLC NAND Flash memory [3]. AEP-LDPC can correct errors more accurately by precisely describing the error phenomena. In this paper, the effects of AEP-LDPC are investigated in a 2Xnm TLC NAND Flash memory with temperature characterization. Compared with LDPC-with-BER-only, the SSD's data-retention time is increased by 3.4x and 9.5x at room-temperature (RT) and 85°C, respectively. Similarly, the acceptable BER is increased by 1.8x and 2.3x, respectively. Moreover, AEP-LDPC can correct errors with pre-determined tables made at higher temperatures to shorten the measurement time before shipping. Furthermore, it is found that one table can cover behavior over a range of temperatures in AEP-LDPC. As a result, the total table size can be reduced to 777kBytes, which makes this approach more practical.

Keywords: NAND Flash memory, solid-state drive (SSD), low-density-parity-check (LDPC), error-correcting code (ECC)

I. INTRODUCTION

Error-prediction low-density-parity-check (EP-LDPC) has been previously proposed for 2-bit/cell multi-level cell (MLC) NAND Flash [1-2]. Although EP-LDPC is effective for MLC NAND Flash [1-2], it is not as effective for 3-bit/cell triple-level cell (TLC) NAND Flash. Therefore, this paper proposes the advanced-error-prediction LDPC (AEP-LDPC) for TLC NAND-based solid-state drives (SSDs) [3]. By more precisely describing the error phenomena, AEP-LDPC can correct errors more accurately at various temperature conditions.

Solid-state drives (SSDs) are replacing hard-disk drives (HDDs) due to their lower power, faster read and compact size. However, SSDs needs to reduce cost in order to expand market share. In a typical SSD, several NAND Flash memories are simultaneously managed by a memory controller. The memory controller applies several techniques to compensate for technology limitations and improve the SSD's performance. Some examples of memory controller functions are wear-leveling [4], garbage collection [5], and error-correcting code (ECC). ECC, in particular, is a significant function to improve reliability. During data write, the ECC circuit encodes the user data and writes parity bits to the NAND Flash's reserved area. Whereas during read, the ECC decoder corrects errors that occur within the NAND Flash by using

several decoding algorithms. In general, ECC decoding performance is improved as the number of parity bits are increased, whereas storage capacity is decreased.

Bose-Chaudhuri-Hocquenghem (BCH) ECC has been used with 2-bit/cell multi-level cell (MLC) NAND Flash memory when the older generations of MLC’s raw bit-error rates (BERs) were acceptably low [6]. However, beyond 20nm, reliability degrades due to stronger neighbor cell coupling/disturb and other interactions [7]. To significantly reduce cost, 3-bit/cell triple-level cell (TLC) NAND Flash memory has been adopted in current SSDs. As a result, SSD reliability is degraded by the lower read margins of TLC NAND Flash [8]. Considering the reliability degradation due to both scaling and multi-level NAND Flash, conventional BCH is not enough for current SSDs. Therefore, to handle low-cost NAND Flash with high BERs, low-density-parity-check (LDPC) is considered the most appropriate approach for next generation ECC [1-2].

In LDPC, data is iteratively decoded based on additional soft (analog) and/or hard (digital) information [9]. The soft information is also called, *log-likelihood ratio* (LLR). LLR(y) is described as follows [10]:

$$\text{LLR}(y) = \ln \frac{p(x = 0 | y)}{p(x = 1 | y)} \quad (2.1)$$

Where x is the transferred data from the host, and y is the received data from TLC NAND Flash memory. Based on the x , the conditional probability is defined as p . By

using the BER, LLR can be represented as follows [2]:

$$\text{LLR}(0) = \ln (1-\text{BER}) / \text{BER} \quad (2.2)$$

$$\text{LLR}(1) = \ln (\text{BER} / (1 - \text{BER})) \quad (2.3)$$

Then, several LDPC decoding algorithms have been proposed (i.e. sum-product (SP) [11], min-sum (MS) [12], bit-flipping (BF) [13]). In general, it is known that soft decoding (SP, MS) is much more effective than hard decoding (BF) [14]. As shown in Fig. 1(a), soft information (LLR) is obtained by extra reads with intermediate references [15], which provides error correction more accurately, but unacceptably long read times. In Fig. 1a's conventional LDPC, soft information derived from V_{Ref} requires seven separate read operations [16]. A faster method, error-prediction LDPC (EP-LDPC) has been developed for MLC NAND Flash, as shown in Fig. 1b [1-2]. EP-LDPC can reduce the read access time by estimating BER from many factors (V_{TH} , W/E cycle, data-retention time, inter-cell capacitive coupling) and compensating for the effects. This paper first describes that, although conventional EP-LDPC is effective for MLC NAND Flash, it is not as effective for TLC NAND Flash. Since V_{TH} differences of programmed states are smaller in TLC NAND Flash compared to MLC, TLC NAND Flash has higher error rates and is more sensitive to program disturb errors. Therefore, this paper proposes advanced error-prediction LDPC (AEP-LDPC)

in Fig. 1c, to correct errors caused by program-disturb, data-retention, as well as floating-gate capacitive coupling [3]. V_{TH} is increased and shifted upwards due to program-disturb [17]. On the other hand, V_{TH} is decreased and shifted downwards due to data-retention [18]. Moreover, floating-gate capacitive coupling also increases V_{TH} due to neighboring cells influence [19].

Compared with conventional EP-LDPC, the advantage of AEP-LDPC is, by precisely describing error phenomena, error correction is more accurate and efficient, with less speed, power or cost overhead. In particular, AEP-LDPC is useful under long term retention. Moreover, this paper evaluates the temperature characterization of AEP-LDPC compared with room-temperature (RT) and 85°C, respectively. Furthermore, it is shown that AEP-LDPC can correct errors with pre-determined tables made at different temperature conditions.

The remainder of this paper is organized follows. The AEP-LDPC decoding method is described in Section II. Next, the measurement results are shown in Section III. In this section, two temperature results, RT, 85°C are compared and discussed. In section IV, all of the pre-determined tables can be made within a shorter time by accelerated high temperature measurements before shipping. Conclusions are given in Section V.

II. ADVANCED ERROR-PREDICTION (AEP)-LDPC SCHEME

A. Architecture of AEP-LDPC

This section describes the architecture of AEP-LDPC. In TLC, three pages (1st/2nd/3rd) are stored in one physical page and there are eight possible V_{TH} states per cell [20]. Each page requires two to three reference levels (V_{Ref}) during read sensing. Page-to- V_{TH} -states mapping is given in Fig. 2. The proposed AEP-LDPC architecture is shown in Fig. 3. During program, user data from the host is encoded by the LDPC encoder. Also, the lowest three states $N_{cellA_initial}$, and the highest state $N_{cellB_initial}$, are counted and these numbers are added to the user data. It is expected that these counts are updated with the write/erase (W/E) cycle. Next, read is described (inside the dashed line of Fig. 3), and three new units are proposed. The retention time estimation unit (Unit1) estimates the BER_{2nd_page} and decides short or long term retention. The short retention time unit (Unit 2) handles short retention cases. The cell-error rate (CER) calculation unit (Unit3) decides the possibility of V_{TH} shift (up /down by one state) and calculates the CER parameters based on the short/long retention. These CER parameters to the LDPC algorithm provide information about which bits are “most likely” to be errors. In LDPC read, decode is iterative, which means that the decoding process may be tried several times ($Decode_{iter}$) before the original data is successfully recovered and

parity check is completed.

B. BER_{2nd_page} Estimation

In AEP-LDPC, the actual data-retention time ($T_{Retention}$) is required for several of the estimations, and can be estimated from BER_{2nd_page} . Therefore, BER_{2nd_page} estimation is described in this section.

During program, the initial number of 2nd page cells are calculated and stored. During ECC decode, the first step is to estimate data-retention time ($T_{Retention}$). BER_{2nd_page} is calculated by re-counting the 2nd page cells and comparing to the initial count. Page-to- V_{TH} -states mapping is given in Fig. 2a. Then, BER_{2nd_page} calculation formula is obtained as follows:

$$BER_{2nd_page} = \{|N_{cellA_initial} - N_{cellA_measured}| + |N_{cellB_initial} - N_{cellB_measured}|\} / N_P \quad (2.4)$$

N_P is the number of all the bits in the 2nd page. Using this formula, BER_{2nd_page} can be calculated easily and precisely.

C. The reason that BER of 2nd page is representative

Although the 2nd page is used to estimate the BER due to data-retention in this case, it should be noted that the 1st page can also be used to estimate the BER, because 1st/2nd pages have only two V_{Ref} 's while the 3rd page has three V_{Ref} 's (Fig. 2). Using a 3- V_{Ref} 's page (Fig. 2b) would result in under-estimation of BER because, although the

errors that occur on $V_{\text{Ref_3rd_1}}$ and $V_{\text{Ref_3rd_3}}$ can be correctly estimated (because N_{cellA} is increased due to “P2” to “P1” error and N_{cellB} is decreased due to “P6” to “P5” error in Fig. 2b), errors occurring on $V_{\text{Ref_3rd_2}}$ cannot be estimated, because there is no observable change of N_{cellC} and N_{cellD} . For example, in N_{cellC} , if the number of cells shifted by data-retention from “P4” to “P3” and “P3” to “P2” are nearly equal, there would seem to be no additional errors on $V_{\text{Ref_3rd_2}}$, and BER would become underestimated. Therefore, the 3rd page which has three V_{Ref} ’s should not be used for BER estimation and BER of 2nd page is representative in this paper.

D. Retention time estimation unit (Unit1)

In Fig. 4a, the retention time estimation flow is shown by considering the $\text{BER}_{2\text{nd_page_Day0}}$ value. In Fig. 4b, and 4c, retention time of $\text{BER}_{2\text{nd_page}}$ is shown at RT and 85°C, respectively. In short term retention, it can be observed that calculated $\text{BER}_{2\text{nd_page}}$ is underestimated compared with measured $\text{BER}_{2\text{nd_page}}$ due to including both program-disturb and data-retention effects, as shown next Fig. 5. Therefore, the region which $\text{BER}_{2\text{nd_page}}$ is below the Day0 value is defined as short retention term. In contrast, the region in which $\text{BER}_{2\text{nd_page}}$ is above the Day0 value is defined as the long retention term. Then, if $\text{BER}_{2\text{nd_page_Day0}} \leq \text{BER}_{2\text{nd_page}}$, the data is considered to be in long term retention and subsequent calculations follow the conventional EP-LDPC

method [1-2]. If $BER_{2nd_page} < BER_{2nd_page_Day0}$, the short term retention calculation method is used (Unit 2). Comparing with both temperature conditions (Fig. 4b, 4c), the short term effect can be ignored at 85°C. This result shows that the thermal emission effect accelerates data-retention error, and the region in which program-disturb error is dominant is extremely short at 85°C.

More details about the BER_{2nd_page} calculation formula, program-disturb and data-retention effects are given in Fig. 5. Since the 2nd page is set by two references, BER_{2nd_page} is calculated by summing the shifted cells in both N_{cellA} and N_{cellB} . Immediately after program, program-disturb's tendency to increase V_{TH} is dominant [17], and the retention effect is negligible. For example, "P2" to "P3" and "P6" to "P7" errors are much higher than "P3" to "P2" and "P7" to "P6" errors, respectively when data-retention time is 1.45ss (Fig. 5). Over time, with data-retention, V_{TH} shifts towards the lower V_{TH} states [18]. Therefore, N_{cell_A} will increase and N_{cell_B} will decrease due to the data-retention effect. When data-retention time is 13 days, it can be observed that "P3" to "P2" and "P7" to "P6" errors are dominant (Fig. 5). However, during short term retention, program-disturb and data-retention push V_{TH} in opposing directions, which means that N_{cell_A} and N_{cell_B} do not change even though errors have actually occurred. As shown in Fig. 5, it can be observed that both errors of V_{TH} increase and decrease exist

when data-retention time is 1.04days. As a result, the BER_{2nd_page} calculation formula will underestimate actual errors.

E. Total BER estimation and short retention time unit (Unit2)

TLC NAND Flash memory has three types of pages (1st/2nd/3rd), and each page's BER behavior is different [21]. For example, the BER of 3rd page is over $1.8\times$ higher than that of 2nd page in 2Xnm TLC [22]. Therefore, when BER_{2nd_page} is applied to all pages, the BER of 3rd page is underestimated about 54%. In order to obtain more accurate LLR, total BER (BER_{Total}) estimation, which averages the three page's BER, is more appropriate compared with applying BER_{2nd_page} to all the pages. As a result, the accuracy of BER_{3rd_page} is improved about 19%, and decoding performance can be improved.

After calculating BER_{2nd_page} , if $BER_{2nd_page} < BER_{2nd_page_Day0}$, total BER uses the Day0 value as shown in Fig. 6. If $BER_{2nd_page_Day0} \leq BER_{2nd_page}$, subsequent calculations follow the conventional EP-LDPC method. Then, data-retention time $T_{Retention}$ can be estimated from BER_{2nd_page} , $N_{W/E}$ and the $T_{Retention}$ table. The $T_{Retention}$ table represents the relationships among BER_{2nd_page} , $N_{W/E}$ and data-retention time. $N_{W/E}$ is the number of W/E cycles when used with a wear-leveling scheme [4].

Subsequently, Total BER (BER_{Total}) is estimated from the BER_{2nd_page} , BER_{1st_page}

table, and BER_{3rd_page} table. As shown in Fig. 7, the BER_{1st_page} table represents the relationships among the proportion of BER_{1st_page} to BER_{2nd_page} , α , $N_{W/E}$ and $T_{Retention}$. Similarly, the BER_{3rd_page} table represents the relationships among the proportion of BER_{3rd_page} to BER_{2nd_page} , β , $N_{W/E}$ and $T_{Retention}$.

The proportion of BER_{1st_page} to BER_{2nd_page} , α , and the proportion of BER_{3rd_page} to BER_{2nd_page} , β , is defined as follows:

$$\alpha(T_{Retention}, N_{W/E}) = \frac{BER_{1st_page}(T_{Retention}, N_{W/E})}{BER_{2nd_page}(T_{Retention}, N_{W/E})} \quad (2.5)$$

$$\beta(T_{Retention}, N_{W/E}) = \frac{BER_{3rd_page}(T_{Retention}, N_{W/E})}{BER_{2nd_page}(T_{Retention}, N_{W/E})} \quad (2.6)$$

Using the BER_{2nd_page} , ‘ α ’ and ‘ β ’ values, BER_{Total} can be calculated as follows [2]:

$$BER_{Total_est} = \frac{(BER_{1st_page} + BER_{2nd_page} + BER_{3rd_page})}{3} \quad (2.7)$$

$$= \frac{(\alpha + \beta + 1) BER_{2nd_page}}{3} \quad (2.8)$$

In Fig. 8, BER_{Total} , estimated by proposed and conventional methods, are shown compared at RT and 85°C, respectively. This figure shows that using BER_{Total_Day0} as the minimum error rate during short term retention (instead of the calculated BER_{Total}) more closely matches the measured BER. Considering two results (RT, 85°C), it can be observed that Unit2 calculation is effective for both RT and 85°C condition.

F. State-Error Rate (SER) and Cell-Error Rate (CER) estimation

The target cell’s BER depends on the V_{TH} of target and neighboring cells. By

considering V_{TH} information, more accurate LLR can be estimated.

After BER_{Total} is estimated, the state-error rate (SER) is estimated from BER_{Total} and state-error ratios as shown in Fig. 9. TLC NAND has eight possible V_{TH} states, and each state has a different SER [22]. This value also depends on the write/erase (W/E) cycle and data-retention time. Fig. 9 shows the calculation in case that the target cell data is "E". After SER is estimated, CER including inter-cell capacitive coupling effect are estimated from the EP-table, which stores cell-error ratios for different neighbor cell V_{TH} 's, as illustrated in Fig. 9. Considering inter-cell capacitive coupling effects improves accuracy because coupling caused by higher V_{TH} 's of neighboring cells can increase the target-cell V_{TH} 's [7], which reduces errors shifted to lower V_{TH} 's due to data-retention. As a result, the target cell's BER is lower when neighboring cells have higher V_{TH} 's. On the other hand, the target cell's BER is higher when neighboring cells have lower V_{TH} 's because coupling effects are not so strong in the case of lower V_{TH} 's [2]. In particular, this coupling effect can be observed when the left and right cell data have higher V_{TH} 's because cells at the same word-line are always programmed simultaneously. As a result, the inter-cell capacitive coupling effect strongly depends on the V_{TH} of neighboring left/right cells. However, this coupling effect cannot be observed when upper and lower cell data have higher V_{TH} 's. By optimizing the order to program

the cell's, the capacitive coupling by upper and lower cells is minimized. By considering the exact coupling effects, more accurate LLR is estimated, which leads to improve error correction capability.

G. Cell-error rate (CER) parameter calculation (Unit3)

In AEP-LDPC, reliability is improved drastically by calculating CER parameters which include program-disturb and data-retention effects. Therefore, a key technique of this work is the calculation of CER parameters to the LDPC decoder (Unit 3). In Fig 10, the proposed AEP-LDPC is compared to the conventional EP-LDPC. In both methods, CER is estimated from BER_{Total} and inter-cell capacitive coupling effects. Moreover, in both methods, V_{TH} is assumed to shift by only one state. (The probability that V_{TH} can shift by two or more states is confirmed, by measurement, to be very low < 0.0002 within the correctable area.) However, conventional EP-LDPC assumes that V_{TH} can shift only downwards due to data-retention error [2]. In reality, immediately after program, the effect of the program-disturb error is stronger than data-retention error in 2Xnm MLC [23]. V_{TH} is shifted upwards when the data is programmed. On the other hand, V_{TH} is shifted downwards as data-retention time is increased. These effects are observed in 2Xnm TLC. Therefore, for better accuracy, AEP-LDPC separates data-retention at RT into two regions, long, when data-retention is dominant, and short, which includes both

the effects of data-retention and program-disturb. Moreover, the data-retention effect can be accelerated due to the thermal emission at high temperature conditions [24]. Since the region which includes both data-retention and program-disturb is extremely short at the high temperature [23], the short term effect can almost be ignored. As a result, AEP-LDPC and EP-LDPC follow the same method at high temperature conditions. Therefore, Unit3 is effective for both RT and high temperature conditions by precisely modeling error phenomena of program-disturb, data-retention and temperature characterization.

H. Memory technology dependencies

Next, the dependence of the proposed techniques on specific memory technologies will be discussed. The BER_{2nd_page} estimation, retention time estimation unit (Unit1), short retention time unit (Unit2), and CER parameter calculation (Unit3) are independent of memory technology and scaling. However, the BER_{2nd_page} estimation and Unit3 should be re-optimized when TLC mapping between 3 pages and 8 V_{TH} levels is changed. On the other hand, $T_{Retention}$, BER_{Total} , SER and CER estimations depend on the memory technology. When memory technology is scaled down, it is expected that the errors will increase. Therefore, pre-determined tables would be needed for each memory technology to estimate $T_{Retention}$, BER_{Total} , SER and CER.

III. MEASUREMENT RESULT AND DISCUSSIONS

A. Measurement setup

In order to evaluate the effectiveness of AEP-LDPC, 2Xnm TLC NAND Flash memory is measured. Before the measurement, user data is encoded to 8KByte LDPC code on the PC. The code rate is 9/10 and 2/3, respectively. The encoded data is written to the TLC NAND and measured data is read by using the memory tester. In order to decode the data, the read data is converted to LLR value by using various pre-determined tables on PC. The input is read data, various measured conditions (temperature, W/E cycle and code rate) and the number of iteration for LDPC decoding. After calculating LLR, LDPC decoding program is executed, and decoded data is outputted. By comparing decoded and correct data, the effectiveness of AEP-LDPC is evaluated on the PC.

Next, LDPC decoder assumption is described. Then, the max iteration number is 30 cycles. If the iteration number is over 30 cycles, the decoding result is "fail". In order to evaluate the latency overhead of iterative decoding, AEP-LDPC decoding latency is calculated to be about 8-32 μ s, assuming a decoding throughput of 10Gbps and 4 iteration cycles [25]. If the code length is 8KByte, this calculation formula is obtained as follows:

$$\begin{aligned}
 \text{Decoding latency} &= \frac{\text{Code length (bit)}}{\text{Throughput (bit/s)} \times \text{Iteration}} \\
 &= \frac{8\text{K} \times 8(\text{bit})}{10\text{G (bit/s)} \times 4(\text{iteration})} \\
 &= 1.6 (\mu\text{s/iteration})
 \end{aligned} \tag{3.1}$$

In addition, BCH ECC is evaluated with the same measurement data encoded by LDPC ECC. BCH ECC can correct t -bit errors in one codeword [26]. Therefore, the decoding capacity of BCH ECC can be estimated by counting the number of errors with the same codeword.

B. Measurement results

In this section, AEP-LDPC measurement results are shown comparing between RT and 85°C. Fig. 11a shows the measured dependence of LDPC Decode_{iter} iterations on data-retention time after 0.5k cycles at RT. Since the number of errors is relatively low in the low iteration cycles and short retention time, both EP-LDPC and AEP-LDPC decoding methods correct errors within a similar number of iterations. In Fig. 11b, when W/E cycle is increased to 4k, more errors occur during short term retention and the advantage of AEP-LDPC over EP-LDPC is clearer. Maximum decode iterations can be reduced by 57%. In long term retention, AEP-LDPC also corrects errors with fewer decode iterations compared with LDPC-with-BER-only.

LDPC-with-BER-only is the reference case of soft decoding LDPC using only the

estimated BER_{Total} (without SER, CER and Unit3) as soft information. This baseline method does not consider state-error rates, inter-cell capacitive coupling effects (Fig. 9), program-disturb and data-retention conditions (Unit3, Fig. 10). After BER_{Total} estimation, BER_{Total} is directly converted to an LLR value.

On the other hand, Fig. 12 shows the measured dependence of $Decode_{ite}$ vs. data-retention time at 85°C, for both AEP-LDPC and EP-LDPC. Although in Fig. 11(b), AEP-LDPC is more effective than conventional EP-LDPC during short term retention at RT, Fig. 12's results shows that the decoding performance of AEP-LDPC and EP-LDPC become similar at 85°C. The explanation for this effect is that short-retention becomes extremely short at 85°C due to the thermal emission effect as shown in Fig. 4(c). Therefore, AEP-LDPC and EP-LDPC are equally effective at 85°C.

Fig. 13a shows AEP-LDPC's measured improvement of the acceptable data-retention time at RT. Acceptable data-retention time is defined as the longest time for which ECC decoding is successful. As a result, AEP-LDPC's acceptable data-retention time is extended by as much as 12x and 3.4x, compared with conventional BCH and LDPC-with BER-only, respectively.

Similarly, Fig. 13b shows the acceptable data-retention time at 85°C. Acceptable data-retention time is extended by as much as 9.5x compared with LDPC-with

BER-only. This result shows that the actual acceptable data-retention time is shorter at 85°C than at RT because the thermal emission effect accelerates data-retention error and raw BER is increased drastically.

Fig. 14 shows the acceptable BER, defined as the highest BER with successful ECC decoding. In Fig. 14a, acceptable BER is increased by 2.8x and 1.8x at RT compared with conventional BCH and LDPC-with BER-only, respectively. Similarly, in Fig. 14b, acceptable BER is increased by 2.3x compared with LDPC-with BER-only at 85°C. This result shows that acceptable BER of AEP-LDPC is usually equal to or better than conventional BCH and LDPC-with BER-only, over a wide range of W/E cycles and temperature conditions.

Usually, BCH ECC is useful just after program because BER is very low in early life of SSD. When W/E cycle and data-retention time is increased, BER is increased drastically. Therefore, AEP-LDPC is used in later part of life and expected to see much overall gain under long term retention.

IV. DECODE WITH PRE-DETERMINED TABLES MADE AT DIFFERENT TEMPERATURE CONDITION

In this section, it is demonstrated that AEP-LDPC can correct errors with a pre-determined table made at high temperature conditions. The benefits are summarized as follows:

- Pre-determined tables can be made within a shorter time by accelerated high temperature measurement before shipping.

- Behavior over a range of temperatures can be reduced down from several tables to a single table.

- Total table size can be reduced from 16MBytes to 777kBytes.

In conventional EP-LDPC, all pre-determined tables are made from measurements before shipping. For example, in order to decode the data for which data-retention time is one year, actual data-retention measurement of one year is needed, which is unacceptably long. For this reason, measurement time reduction is investigated in this section. In general, data-retention error is accelerated due to the thermal emission effect at higher temperatures. If AEP-LDPC decoding by pre-determined tables from high temperature measurement is possible, measurement time before shipping can be drastically shortened.

Moreover, it is found that all temperature measurement data can be decoded with only one kind of table. In conventional EP-LDPC, all pre-determined tables are needed for each temperature. Therefore, in order to cover 20 temperatures, the total table size is approximately 16MBytes. However, AEP-LDPC requires only one kind of temperature table and no thermal sensor. Then, total table size can be reduced to 777kBytes, and this

table can be stored in the TLC NAND Flash without capacity overhead. Therefore, this method becomes more practical.

The total table size (S_{Total}) is calculated as follows [2]:

$$S_{\text{Total}} = S_{\text{EP-table}} + S_{\text{TRetention_table}} + S_{\text{BER_1st_page_table}} + S_{\text{BER_3rd_page_table}} \quad (4.1)$$

$$S_{\text{EP-table}} = W \times N_{\text{VTH}}^2 \times N_{\text{Neighboring_cell}} \times N_{\text{TRetention}} \times N_{\text{W/E}} \quad (4.2)$$

$$S_{\text{TRetention_table}} = W \times N_{\text{TRetention}} \times N_{\text{W/E}} \quad (4.3)$$

$$S_{\text{BER_1st_page_table}} = W \times N_{\text{TRetention}} \times N_{\text{W/E}} \quad (4.4)$$

$$S_{\text{BER_3rd_page_table}} = W \times N_{\text{TRetention}} \times N_{\text{W/E}} \quad (4.5)$$

In above formula, W is the bit width of each stored value, N_{VTH} is the number of V_{TH} states, and $N_{\text{Neighboring_cell}}$ is the number of neighboring cells. $N_{\text{TRetention}}$ and $N_{\text{W/E}}$ are the numbers of the measurement points of $T_{\text{Retention}}$ and W/E cycle, respectively.

The EP-table, $T_{\text{Retention}}$ table, $\text{BER}_{1\text{st_page}}$ table and $\text{BER}_{3\text{rd_page}}$ table store the cell-error ratio, the $\text{BER}_{2\text{nd_page}}$, the proportion of $\text{BER}_{1\text{st_page}}$ to $\text{BER}_{2\text{nd_page}}$, and the proportion of $\text{BER}_{3\text{rd_page}}$ to $\text{BER}_{2\text{nd_page}}$, respectively. In order to store these values, it is needed to consider the maximum bit-error number in a block. If page size is 8KByte and 258 pages are stored in a block, a block size and the maximum error number are approximately 2MBytes. Therefore, 24bits are needed for each stored value. Assuming that W is 24, N_{VTH} is 8 (3bit/cell), $N_{\text{Neighboring_cell}}$ is 4 (upper/lower/left/right cells),

$N_{\text{TRetention}}$ is 100, and $N_{\text{W/E}}$ is 10, S_{Total} is approximately 777kBytes.

This table size is negligibly small compared with 64Gbit TLC NAND Flash memory. If this table is used as the storage, the number of parity bit is increased only about 6bits for each 8KByte codeword. Therefore, decoding performance is almost the same even though pre-determined tables are used as the storage.

To illustrate the above points, in this section, two temperature conditions, RT and 85°C, are compared, and tables are made for each temperature condition. Fig. 15 shows the measured $\text{BER}_{2\text{nd_page}}$ vs. data-retention time at RT and 85°C, respectively. Based on the $\text{BER}_{2\text{nd_page}}$, data-retention time ($T_{\text{Retention}}$) can be estimated. Note that under both temperature conditions, $\text{BER}_{2\text{nd_page_Day0}}$ is almost the same. However, data-retention error increases faster at 85°C. Therefore, for a given $T_{\text{Retention}}$, the equivalent $T_{\text{Retention}}$ ($T_{85\text{degC}}$) can be estimated from the same $\text{BER}_{2\text{nd_page}}$ at 85°C. A table of $T_{\text{Retention}}$ and equivalent $T_{85\text{degC}}$ is made from the measurement results.

First, $\text{BER}_{2\text{nd_page}}$ estimation is described. Fig. 16 shows the measured $\text{BER}_{2\text{nd_page}}$ vs. data-retention time at RT. In $\text{BER}_{2\text{nd_page}}$ estimation, temperature does not need to be considered, because the number of errors is directly obtained from read data, not predetermined tables. Moreover, the decision of short/long term is also shown in Fig. 16. Short/long term effects are dominant when the $\text{BER}_{2\text{nd_page}}$ is below/above the Day0

value, respectively. In Fig. 16, $BER_{2nd_page_Day0}$ is almost the same at both RT and 85°C. Therefore, the decision of short/long term can be estimated, regardless of the temperature.

Next, based on the 85°C table, BER_{Total} estimation is described. Fig. 17a shows the measured BER_{Total} , the estimated BER_{Total} with the RT table and the estimated BER_{Total} based on the 85°C table when the temperature condition is RT. BER_{Total} estimation uses α and β values derived from the BER_{1st_page} and the BER_{3rd_page} tables based on W/E cycle and $T_{Retention}$ (Fig. 7). In general, these table values vary with temperature. However, this figure shows that BER_{Total} is similar, by using the equivalent T_{85degC} values.

The reason that BER_{Total} estimation is successful is explained further in Fig. 17b. Referring to Fig. 15, both $T_{Retention}$ values (T_{RT} , T_{85degC}) which are derived from RT and 85°C tables are estimated by using same BER_{2nd_page} value. Fig. 17b compares $T_{Retention}$, α , β and BER_{Total} when BER_{2nd_page} is almost the same. Then, it can be observed that estimated α and β values are similar, even though $T_{Retention}$ is different, as long as BER_{2nd_page} is almost the same. Therefore, BER_{Total} can be successfully estimated, even with accelerated temperature measurement.

Similarly, SER and inter-cell capacitive coupling effect are compared at RT and 85°C.

Fig. 18 shows the measured SER when BER_{2nd_page} is almost the same compared with RT and 85°C. Data-retention time is 41days at RT, and 1.04days at 85°C, respectively. It is seen that each state has almost the same BER except the 'P3' and 'P7' state compared with RT and 85°C. It can be observed that the 'P3' SER at 85°C is larger than that at RT. However, although SER is slightly high by using 85°C table instead of RT table (Fig. 18), the decoding result is similar as shown in Fig. 20.

Fig. 19 shows the target cell-error ratio compared at RT and 85°C. Data-retention time and W/E cycles are the same as for Fig. 18. It can be observed that the target cell-error-ratio (CER) depends only on the inter-cell capacitive coupling effect when BER_{2nd_page} is almost the same. Thus, CER does not depend on the temperature.

Fig. 20 shows the measured decoding iterations using the RT table and the 85°C table. This figure shows decode iterations do not change significantly, even if AEP-LDPC decoding uses the 85°C table instead of the RT table. This is because BER_{Total} , SER and cell-error ratio parameters can also be estimated as shown in Fig. 17, 18 and 19. As a result, the latency overhead is negligibly small by using the 85°C table.

Thus, by considering BER_{2nd_page} instead of data-retention time, AEP-LDPC can correct errors with pre-determined tables made at high temperature conditions, which can accelerate the measurement time to make all tables before shipping. Furthermore, it

is shown how AEP-LDPC can correct errors measured at various temperature by using only one kind of temperature table without the need for a thermal sensor. As a result, the total table size can be reduced to 777kBytes, which allows more practical implementation.

V. CONCLUSION

The key features of AEP-LDPC at RT are summarized in Table I. Compared to conventional BCH and LDPC-with BER-only, data-retention time is extended by 12x and 3.4x, respectively. Similarly, acceptable BER is increased by 2.8x and 1.8x. Moreover, the features of AEP-LDPC at 85°C are summarized in Table II. Compared to conventional LDPC-with-BER-only, data-retention time is extended by 9.5x, and acceptable BER is increased by 2.3x, respectively. Also, compared to EP-LDPC, short retention error correction is provided, and maximum decode iterations are reduced by 57%. Furthermore, AEP-LDPC decoding with pre-determined tables made at higher temperature conditions is investigated. It is demonstrated that all of the pre-determined tables can be made with shorter measurement times by accelerated high temperature testing. Also, AEP-LDPC requires only one kind of temperature table, which allows the total table size to be reduced to 777kBytes. Thus, a highly reliable SSD operable under a range of temperatures can be realized with low-cost TLC NAND Flash memory.

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Fig. 1

Fig. 2

Fig. 3

Fig. 4

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Fig. 7

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Fig. 9

Fig. 10

Fig. 11

Fig. 12

Fig. 13

Fig. 14

Fig. 15

Fig. 16

(b)

Temperature	RT	85degC
BER _{2nd_page} (a.u.)	0.49	0.47
$T_{\text{Retention}}$	41days	1.04days
α (BER _{1st_page} / BER _{2nd_page})	1.18065	1.38699
B (BER _{3rd_page} / BER _{2nd_page})	0.74285	0.89919
BER _{Total} (a.u.)	0.4775	0.51483

Fig. 17

Fig. 18

Fig. 19

Fig. 20

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Table 1: Summary of AEP-LDPC scheme at RT.

Table II: Summary of AEP-LDPC scheme at 85°C.

@RT		Conventional BCH	LDPC with BER only	EP-LDPC	AEP-LDPC
SSD lifetime (Code rate : 2/3)	$N_{W/E} : 4k$	2 days	7 days	24 days	24 days (x12 vs. BCH) (x3.4 vs. BER only)
	$N_{W/E} : 6k$	Fail	1.3 days	Fail	1 days
Acceptable BER (Code rate : 2/3)	$N_{W/E} : 4k$	1.5 %	2.3 %	4.0 %	4.0 % (x2.8 vs. BCH) (x1.8 vs. BER only)
	$N_{W/E} : 6k$	Fail	2.2 %	Fail	2.1 %
Decode iterations	Short retention (Code rate :2/3 $N_{W/E} : 4k$)	-	7 iterations	14 iterations	6 iterations (-14% vs. BER only) (-57% vs. EP-LDPC)
	Long retention (Code rate : 9/10 $N_{W/E} : 0.5k$)	-	25 iterations	12 iterations	12 iterations (-52% vs. BER only)

Table I

@85degC	Conventional BCH	LDPC with BER only	EP-LDPC	AEP-LDPC
SSD lifetime (Code rate : 2/3) $N_{W/E} : 1k$	Fail	2.2 days	20 days	20 days (x9.5 vs. BER only)
Acceptable BER (Code rate : 2/3) $N_{W/E} : 1k$	Fail	1.8 %	4.1 %	4.1 % (x2.3 vs. BER only)
Decode iterations (Code rate : 2/3) $N_{W/E} : 1k$	-	17 iterations	7 iterations	7 iterations (-59% vs. BER only)

Table II