Fabrication and characterization of sub-micron $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-i-n diodes

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Abstract

The impact of scaling on off-state current of p-i-n diodes is studied. A sub-micron p-i-n diode exhibits a dominating surface component of leakage current. Variation in i-layer thickness has an impact on bulk leakage. Bulk leakage scales with cross-sectional area of the diode and surface leakage has been controlled using surface treatments to give ultra low leakage currents of 210 fA for a device of cross sectional area of $0.44 \mu\text{m}^2$. Devices of 100 nm i-layer thickness show an average bulk and surface current densities of $100 \text{ mA}/\text{cm}^2$ and $150 \text{ fA}/\mu\text{m}$, respectively.

Keywords: sub-micron, III-V, $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, p-i-n

1. Introduction

A tunneling field-effect transistor (TFET) is a strong contender to replace the MOSFET in the field of low-power electronics because of band-to-band tunneling (BTBT) of carriers as the dominating transport mechanism that theoretically enables a sub-60 mV/decade subthreshold swing [1]. A TFET operates as a reverse-biased p-i-n diode with a gate over the intrinsic region. A p-i-n diode is a p-n junction with an intrinsic region between the p-layer and the n-layer. The p and n regions are degenerately doped, so as to enable BTBT upon application of gate bias. These regions form the source and drain, respectively, of an nTFET, in which electrons are the majority charge carriers. The opposite holds true for a pTFET. The intrinsic region is undoped that forms the channel region between the source and drain. The off-state current, or leakage current, of a TFET can therefore be defined as the current flowing in a p-i-n diode in reverse bias mode.

An Esaki tunnel diode is a p-i-n diode with an intrinsic region on the order of the space charge region between the degenerately doped p and n layers. The

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majority of processing background for this study has been developed by Pawlik *et al.* [2] during his work on sub-micron Esaki diodes. Benz *et al.* demonstrated the transition of breakdown mechanisms from impact ionization in tunnel diodes to a soft breakdown of BTBT and trap-assisted tunneling (TAT) in p-i-n diodes with the increase in i-layer thickness [3, 4, 5].

Traditionally, p-i-n diodes have been used as photodetectors in the field of optoelectronics because of their fast switching capabilities. In order to maximize photon absorption, the dimensions were of the order of tens of μm in cross-section and i-layer thickness to the order of 1–5 μm . Because of a large cross-sectional area, leakage current was characterized to flow through the bulk of the device. When implementing for a TFET logic, the p-i-n needs to be scaled down by a factor of 100–1000 in the cross-sectional area and a factor of 10–50 in the i-layer thickness, which brings forth a surface component of leakage in addition to the aforementioned bulk leakage. With a reduction in size, the area to perimeter ratio of a device decreases, increasing the impact of surface states on I_0 tremendously.

Until now, TFETs have been realized on large area p-i-n diodes [6, 7], however, it is essential to characterize sub-micron TFET and p-i-n structures which is critical for integration of TFETs into modern VLSI/UVLSI circuits [8, 9]. The major problem plaguing the TFET device is the tradeoff between on and off-state performance. When a TFET shows a MOSFET-like on-state current, it suffers heavily in terms of leakage and a poor SS [10]. Looking at individual factors, a higher I_{on} can be achieved by increasing the tunneling probability of charge carriers, which increases with a reduction in effective mass and a decrease in the energy gap of the material [1]. In the widely used $\text{In}_x\text{Ga}_{1-x}\text{As}$ material system, the bandgap reduces with an increase in x (between 0 and 1) [11, 12]. Another way of boosting I_{on} is by using heterojunctions [10, 13] or pocket doping at the source-channel interface [7, 14, 15] that reduce the effective barrier for the charge carriers to tunnel. In these devices, bulk leakage can be controlled by controlling the electric field in the device, whereas surface leakage is dominated by conductive oxides and impurities at the interface.

Surface states due to material and process related issues have been shown to cause a shunt leakage current for InSb and InAs p-i-n structures [16, 17] increasing I_0 of the devices and decreases their sensitivity. Two experiments performed by Chee *et al.* [18] and Xu *et al.* [19, 20] showed the tendency of accumulation of In and Ga at the surface, which is a cause of high interface states. It has been shown that unless properly passivated, the mesa sidewall has a large number of dangling bonds and also oxidizes when exposed to atmosphere creating In_xO_y and Ga_xO_y , leading to Fermi level pinning at the surface.

This Fermi level penetrates into the conduction band at the surface causing the electrons to occupy quantized states. This inversion layer has a shunt path to the n-type drain and forms a sidewall p-n junction at the p^{++}/i interface. Tunneling occurs when the p-side is heavily doped and the energy of electrons in the p-side overlaps the empty states in the conduction band of the n-region causing a shunt path for leakage current without any gate bias [21]. Low temperature characterization done by Lin *et al.* [22] showed the impact of surface

leakage on the reverse-bias current in an InAs p-i-n diode, by depleting the surface of charge carriers.

This study reports on the fabrication and characterization of sub-micron homojunction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-i-n diodes and reports off-state current of the order of 100 fA. Experiments done in this study will be focused on the dimensional dependence of leakage current in sub-micron p-i-n diodes. Whether bulk dark current still dominates, or does surface leakage take over at small dimensions is expected to be understood from this study.

2. Experiment

In this study, homojunction $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ p-i-n structures (D1, D2 and D3) were grown using molecular beam epitaxy (MBE) on an InP substrate. D1 had a 300 nm p^{++} source, 50 nm i-region and a 30 nm n^{++} drain. D2 had a 300 nm p^{++} source, 100 nm i-region and a 30 nm n^{++} drain. D3 had a 300 nm p^{++} source, 100 nm i-region and a 300 nm n^{++} drain (Fig. 1). All the three structures have similar doping levels.

30 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	n^{++}
50 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	i
300 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	p^{++}
Substrate	InP	S.I.

(a)

30 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	n^{++}
100 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	i
300 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	p^{++}
Substrate	InP	S.I.

(b)

300 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	n^{++}
100 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	i
300 nm	$\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$	p^{++}
Substrate	InP	S.I.

(c)

Figure 1: Layer structures used in this study. (a) D1: 50 nm i-region, (b) D2: 100 nm i-region, (c) D3: 100 nm i-region, 300 nm drain

200 nm of Mo was deposited as top metal in a DC sputter tool. The same process was then repeated on the backside of the wafer to contact the bottom substrate using Mo. The top metal of the vertically grown diodes was patterned using a negative tone chemically amplified resist, n-LOF 2020 by e-beam lithography (EBL). The resist pattern was transferred to the Mo layer by a SF_6 plasma in a RIE chamber. Using the etched Mo as a hard mask, the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ mesa etch was performed using a 20:1 citric acid: H_2O_2 solution [23] to etch the semiconductor, stopping at the tunneling interface of p^{++} and i-layer. D1 was etched for 73 seconds, D2 was etched for 118 seconds and D3 was etched for 6 minutes.

The samples were coated with BCB and cured in a N_2 ambient at 250 °C for 60 min. The BCB was etched back until the top metal was exposed for Level 2 lithography. The probe pads were defined using EBL with a double resist stack of positive tone resist ARCH-8250 on liftoff resist LOR-5A. After the lithography step, 200 nm of Mo was deposited using the same process as used for top and bottom metal, after which it was lifted off in a Remover PG solution heated at 75 °C.

3. Result and Discussion

Electrical testing of the devices was performed using a Keithley 4200 Semiconductor Parameter Analyzer. To standardize leakage current, I_0 , for a proper comparison of different device structures, current was observed at a reverse bias of 0.5 V. The layout of devices on the mask set was designed such that devices of 11 different sizes were tested. A model was developed that represents measured current as the sum of the cross-sectional area (A) times bulk current density (J_B) and perimeter (P) times surface current density (J_S) [24].

$$I = A \cdot J_B + P \cdot J_S \quad (1)$$

Assuming a square device (edge length W μm), the equation can be represented as,

$$I = W^2 \cdot J_B + 4W \cdot J_S \quad (2)$$

Dividing both sides by W ,

$$\frac{I}{W} = W \cdot J_B + 4 \cdot J_S \quad (3)$$

This is the equation of a straight line where measured current per unit edge length, I/W can be plotted against edge length, W of the device. The slope of the line gives bulk current density and the y-intercept gives the surface current density. This method for extraction of the different components of leakage current is a first order approximation and isolates the surface and bulk mechanisms such that it does not account for leakage mechanisms that are common to both the bulk and the surface. In the absence of other analysis methods, this is a way to qualitatively estimate and compare leakage in different p-i-n structures.

Figure 2: (a) P-i-n fabrication process flow. (b) SEM micrograph of D1 after citric acid mesa etch showing 200 nm Mo on an 80 nm etched mesa. Undercut (both sides) is of the order of the depth of the etch.

Fig. 2b shows a SEM micrograph of device D1 after mesa etch. The mesa height etched was 80 nm (30 nm n^{++} + 50 nm i-layer). The undercut was measured to be 110 nm (55 nm on each side). For a top Mo square of dimension

$500 \times 500 \text{ nm}^2$, the effective cross section of the device is reduced to roughly $400 \times 400 \text{ nm}^2$ (reduction by 36%). This number may vary significantly based on the thickness of the layers to be etched, the size of the top Mo contact and the starting substrate/buffer layers of the sample. It is, therefore, necessary to analyze the samples individually and determine the undercut.

Figure 3: I-V curve of D1 (triangles) and D2 (dots) depicting different leakage current and device breakdown mechanisms.

Typical I-V characteristics of D1 (50 nm) and D2 (100 nm) are shown in Fig. 3. In the forward bias regime, the two devices show a similar curve, but D1 has a larger current because of a larger diode area. In the reverse bias, D1 has a leakage floor 2 orders of magnitude higher than D2, defined by SRH G-R [25]. With an increase in bias, the carriers hop over the energy gap assisted by a defect state, which is termed as trap-assisted tunneling (TAT). With a further increase in bias, the carriers do not require a middle state and directly tunnel from the valence to the conduction band (BTBT) [6]. A further increase in bias would lead to permanent device breakdown in the form of impact ionization.

As the i-layer thickness is increased from 50 to 100 nm in D2, the leakage mechanisms are shifted towards a higher (reverse) bias range, as the field across the intrinsic region is reduced (to half, in this case). By looking at a typical operating point of -0.5 V , D2 shows 4 orders of magnitude lower leakage than D1. This shows that bulk leakage can be reduced by increasing the i-layer thickness. However, increasing the thickness to a very high value may give rise to other

problems, namely, devices of high aspect ratio that may be physically weak, an increase in process variations, and an additional small parasitic resistance in the device.

Figure 4: I_0 (at -0.5 V) vs. cross-sectional area of the diode for D1 (50 nm) and D2 (100 nm). Sub-micron p-i-ns can be seen to the left of $1 \mu\text{m}^2$ on the x-axis.

Fig. 4 shows I_0 scaling with cross-sectional area of the p-i-n for D1 and D2. For a large area device, the current scaled linearly with the cross-sectional area. However, as the dimensions approached $0.5 \mu\text{m}^2$, the current fell off the trend and saturated. For devices at these dimensions, the perimeter to area ratio is much higher than those at the extreme right edge of the plot in Fig. 4, leading to an increased surface impact.

Fig. 5 shows I-V characteristics of D3 with a 100 nm i-region tested before and after a 60 s HCl clean. The HCl clean is 10:1 solution of DI H_2O :HCl, which is used to remove surface oxidation (In_xO_y and Ga_xO_y) on $\text{In}_x\text{Ga}_{1-x}\text{As}$ surfaces. The clean is performed before mesa encapsulation by BCB to remove any surface oxidation.

At low values of forward bias, pre-clean devices show an increase in current (increase in ideality factor), which is characteristic of a TFET at low gate bias, indicative of channel formation at the surface. Prior to the clean, I_0 at -0.5 V was observed at 1×10^{-8} A which reduced to 8×10^{-11} A after the HCl clean. The I-V curves of the devices before the clean indicate TAT from ~ -0.2 V to -0.7 V and then a clear rise in current after that, characteristic of BTBT [26].

Figure 5: I-V curve of D3 before (black, dot-dash) and after (blue, solid) a 60 s HCl clean. Trap-assisted tunneling and BTBT suppressed in the sample cleaned with HCl.

This also suggests that along with the bulk, these two leakage mechanisms play a significant role at the surface as well.

Fig. 6a and 6b show I_0 scaled per cross-sectional length against cross-sectional length of the diode for D1 (black), D2 (red) and D3 (blue) to obtain a straight line, according to Eq. 3. The different slopes of the datasets are an indication of different degrees of bulk leakage in the three samples. While D1 has a higher J_B because of a thin i-region, D3 shows a smaller slope than D2 because of a thicker 300 nm n^{++} drain capping the i-region (as compared to a 30 nm n^{++} drain in D2) that makes the I_0 more forgiving to processing induced damages. Extracted J_B for D1, D2 and D3 are 16 A/cm², 2.3×10^{-3} A/cm² and 1.04×10^{-4} A/cm², respectively. The intercept of D2 and D3 is roughly the same, accounting for a similar J_S because of the same i-layer thickness. Extracted J_S (y-intercept divided by 4) of D1, D2 and D3 are 0.5×10^{-10} A/ μ m, 1×10^{-13} A/ μ m and 1.5×10^{-13} A/ μ m, respectively.

Using the model, for a device of cross-sectional length of 660 nm, 1 μ m and 1.44 μ m, I_0 was calculated to be 832 fA, 1.6 pA and 2.9 pA, respectively. From measurements of device D3, median I_0 for the same devices was measured to be 1 pA, 1.7 pA and 2.2 pA, respectively. The deviations may be a result of the square-device approximation of the p-i-n diode, that would affect the value of

Figure 6: Current per unit edge length of the mesa cross-section vs the mesa length. Comparison of bulk and surface leakage components in (a) D1 and D2, (b) D1 and D3.

I_0 most dramatically.

4. Conclusion

This study reports leakage current in sub-micron p-i-n diodes of varying intrinsic layer thicknesses. A first-order model to extract leakage was also suggested that estimated a bulk and surface current densities of 16 A/cm^2 and $50 \text{ pA}/\mu\text{m}$, respectively, in the device with 50 nm i-layer thickness, and $1.04 \times 10^{-4} \text{ A/cm}^2$ and $150 \text{ fA}/\mu\text{m}$, respectively, in the device with 100 nm i-layer thickness. It was shown that tunneling (BTBT and TAT) is both a bulk and a surface phenomenon and while bulk leakage is a scalable component, surface leakage can be reduced significantly by surface treatments.

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