A Scaling Scenario of Asymmetric Coding to Reduce Both Data Retention and Program Disturbance of NAND Flash Memories

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Abstract

An optimized asymmetric coding strategy is proposed to improve the reliability of the NAND flash memories. The previously reported asymmetric coding reduces the data-retention error by decreasing the population of the V_{TH} state which has higher error rate, and is measured on 4Xnm NAND flash memory [1]. In [2], by increasing the number of the lowest V_{TH} state, the proposed asymmetric coding strategy reduces the V_{PGM} disturbance, and alleviates the floating-gate (FG)-FG coupling. And also, the program-disturb bit error rates (BERs) in 2Xnm, 3Xnm, and 4Xnm NAND flash memories are reduced by 71%, 73%, and 89%, respectively. In this paper, the effect of asymmetric coding on the data-retention error is investigated in 2Xnm NAND flash memory. From the measured results, the proposed asymmetric coding effectively increases the population of the lowest V_{TH} state which has no data-retention error. The data-retention BERs in 2Xnm, 3Xnm and 4Xnm NAND are decreased by 17%, 52% and 70%, respectively.

Keywords: NAND flash memory, asymmetric coding, reliability, program disturb error, data-retention error

I. INTRODUCTION

The NAND flash memories in solid-state drives (SSDs) are continuously scaled down to realize the high storage capacity and low-cost [3]. Recently, the feature size of NAND flash memories has reached 16nm [4]. However, NAND flash memories are suffering from the aggressive scaling caused reliability degradation [5]. To overcome the reliability problems, the asymmetric coding [1] and other error-correction techniques [6-8] have been proposed to realize the highly reliable SSDs. The asymmetric coding improves the data-retention bit error rate (BER) by reducing the population of the V_{TH} state which has higher error rate after data retention. By using the asymmetric coding, either the population bit “0” or bit “1” is possible to be increased. Fig. 1 shows the algorithm of the asymmetric coding for the case of 4-bit code length in which the amount of “1”s are increased [1]. In detail, data in the codeword are bit-flipped by setting the flag bit to “1”, if the amount of “0”s in the codeword is equal to or larger than the threshold (2 bits in this case). Otherwise, data in the codeword is not flipped and the flag bit is “0”, because the population of data “1” is larger than “0”. In this way, the asymmetric coding can increase the population of “1”s in the programming data so that the bit errors of NAND flash memory can be decreased [1].

In addition to [2], this work proposes an optimized asymmetric coding strategy for program-disturb error in 2Xnm, 3Xnm and 4Xnm NAND flash memories in the following perspectives: data-retention error of MLC NAND flash memory cells in each V_{TH} state, analyses of the asymmetric-coding effect on the data-retention error by increasing the population of different V_{TH} state, and the proposed asymmetric coding for the data-retention error.

Thus, this paper evaluates the effects of the asymmetric coding in the 2X-4Xnm NAND flash memories for the data-retention error and the program-disturb error. One chip in each

generation (2X-4Xnm) is tested. The error rate of each V_{TH} state with both the random pattern and the asymmetric coding is analyzed. To improve the reliability of the NAND flash memories, an optimized asymmetric coding strategy is proposed. From the experimental results, by using the proposed coding method, the program-disturb BERs in 2Xnm, 3Xnm and 4Xnm NAND flash memories are reduced up to 71%, 73% and 89%, respectively. For data-retention error, the BERs in 2Xnm, 3Xnm, and 4Xnm NAND flash memories decrease 17%, 52% and 70%, respectively.

This paper is organized as follows. The multi-page cell architecture is explained in Section II to discuss the strategies of the asymmetric coding. The state-error rate of NAND flash memory cells is analyzed. In Section III, the program-disturb error rates of memory cells in each V_{TH} state are analyzed by using the random pattern and the asymmetric coding. In addition, an optimized asymmetric coding for the program-disturb error is proposed. The measurement results in 2Xnm, 3Xnm and 4Xnm NAND flash memories with the proposed asymmetric coding for the program-disturb error are shown. In Section IV, the data-retention error by using asymmetric coding is analyzed. Moreover, the most effective asymmetric coding strategy is proposed from the experimental results. The proposed asymmetric coding is applied to reduce the data-retention error in 2X to 4Xnm NAND flash memories. Finally, the conclusion is given in Section V.

II. Reliability of NAND Flash Memory

A. Multi-page Cell Architecture

The multi-level cell (MLC) NAND flash memory stores 2 bits per cell. One of them belongs to the upper page and the other belongs to the lower page. There are two programming methods for MLC NAND flash memory, the full-sequence programming and the multi-page cell architecture [9-10]. In the full-sequence programming, all bits in a cell are programmed simultaneously. In the case of the multi-page cell architecture, one bit in a MLC cell is programmed during each programming operation. The multi-page cell architecture is used in MLC NAND flash memories to accelerate the read/write performance. The multi-page architecture is shown in Fig. 2. First, the memory cells in the lower page are programmed and the memory cells are divided into two V_{TH} states. Then, the upper page is programmed and the memory cells are divided into four V_{TH} states. As a result, the data pattern of the MLC NAND flash memory cell is represented as “11”, “01”, “00”, and “10”, from the lowest to the highest V_{TH} state.

B. The Reliability of NAND flash memory

As the NAND flash memories is scaled down, the program-disturb error and the data-retention error are increased and the reliability of NAND flash memories is degraded [1]. The program-disturb error is caused by the unexpected electron injection from the channel to the floating gate because of the programming voltage (V_{PGM}), pass voltage (V_{PASS}) disturbances and the hot electron injection by the gate-induced drain leakage (GIDL) [11-14]. Thus, the program-disturb error corresponds to the V_{TH} increase, e.g. “11” $\rightarrow$ “01”, “01” $\rightarrow$ “00”, or “00” $\rightarrow$ “10” (Fig. 3).

The data-retention error is caused by the electron ejection from the floating gate due to stress-induced leakage current (SILC) and random-telegraph noise (RTN) [15-17]. For that reason, the data-retention error corresponds to the V_{TH} decrease, e.g. “01” → “11”, “00” → “01” and “10” → “00” (Fig. 4).

The program-disturb error rate and the data-retention error rate in each V_{TH} state (state-error rate) are measured on 4Xnm, 3Xnm and 2Xnm NAND flash memories respectively (Fig. 5-6). The state-error rate is calculated as in formula (2.1):

$$\text{State error rate} = \frac{\text{Number of error memory cells in each } V_{TH} \text{ state}}{\text{Total number of memory cells in each } V_{TH} \text{ state}} \dots\dots\dots (2.1)$$

For the measurement, 10k write/erase cycles are first applied, followed by the random-pattern programming. All state-error rates for the program-disturb error are increased, as feature size of NAND flash memories is reduced (Fig. 5). In case of the data-retention error, “00” → “01” error and “10” → “00” error are increased to scale down the NAND flash memories (Fig. 6). In addition, the measurement results show the different state-error rate in each V_{TH} state. This would be caused by the erratic tunneling due to the RTN or the hole trapping [18-19]. If the clusters of the positive charges are within the tunnel oxide, the FN tunneling operation becomes anomalous. On the other hand, when the hole trapping is increased, the FN tunneling current is increased.

III. Proposed Asymmetric Coding Strategy for Program-Disturb Error

A. Analyses of Error Rate of Each V_{TH} State for Program-Disturb Error

In Fig. 7, by using the asymmetric coding, the population of each V_{TH} state is increased respectively, and the state-error rates are compared including the asymmetric coding and the random case without asymmetric coding. Fig. 7(a) shows the state-error rate comparison with 3Xnm NAND flash memory. 10k write/erase cycles are first applied. Increased error can be found by increasing either the population of state “00” or state “10”. On the other hand, for 2Xnm NAND flash in Fig. 7(b), if the population of the highest V_{TH} (“10”) state increases, all state-error rates are increased and larger than the state-error rates of random pattern. It can be concluded that the state-error rate in 2X/3Xnm NAND flash memories get worse if the “10” population increases. This is caused by the increased program-voltage stress and the large floating-gate (FG)-FG capacitive coupling. Higher program voltage accelerates the hot electron injection from substrate to the floating gate and increases the V_{PGM} disturbance [20]. The FG-FG coupling increases the V_{TH} of the neighboring memory cells [21-23]. These mechanisms cause the increment of program-disturb error. On the other hand, if the populations of lower V_{TH} state (“01” or “11”) is increased, for each state-error on 3Xnm NAND flash in Fig. 7(a) and 2Xnm flash in Fig. 7(b), the error rates are smaller than the state-error rate by using then random pattern. This is due to the reduction of both the FG-FG coupling and V_{PGM} disturb.

B. Proposed Asymmetric Coding Strategy for Program-Disturb Error

The proposed asymmetric coding is shown in Fig. 8. The population of bit “1” in both lower and upper page are increased by asymmetric coding, so that the population of “11” is increased to reduce the program disturb, V_{PGM} disturb and FG-FG coupling (Fig. 8).

Fig. 9 shows the relations of flag bit overhead and the maximum population in four V_{TH}

states. In this paper, the state of “11” is decided to be increased as previous discussed. The reliability of NAND flash memory can be improved by enhancing the asymmetry of stored data. However, the flag bit caused data overhead is also increased. For example, if the code length of the asymmetric coding is 16 bits, the maximum population is 36% and the flag is one bit and the overhead is 6%. On the other hand, if the code length of the asymmetric coding is 2 bit, the maximum population and the flag overhead are 56% and 50%, respectively. As a result, the area of the NAND flash memory array should be increased to enhance the effect of the asymmetric coding.

Fig. 10 shows the random pattern based average page-program time by measuring the proposed asymmetric coding on 256 pages of 2Xnm NAND flash memory. 10k write/erase cycles are firstly applied before the asymmetric coding measurement. The program time by using the random pattern is almost equal to the one with the proposed asymmetric coding pattern. Thus, if the distribution of the V_{TH} states is changed by the proposed asymmetric coding, there is no increase of the program time.

Fig. 11 compares the program-disturb bit error number per page by using the random pattern and the proposed asymmetric coding. The code length of the proposed asymmetric coding is 2 bit. In both of the upper page and the lower page, the bit-error number is decreased by applying the proposed strategy. The bit-error numbers in the upper page and the lower page are decreased by 82% and 67%, respectively.

“11” state is the V_{TH} state which has the lowest state-error rate. If the “11” population is increased, the V_{PGM} disturb and the FG-FG coupling are also reduced. The proposed asymmetric coding strategy increases the population of “11” state. Fig. 12 shows the measured program-disturb BER in 2Xnm, 3Xnm and 4Xnm NAND flash memory with the random pattern and the proposed asymmetric coding. The BER is calculated as formula 3.1:

$$\text{Bit error rate (BER)} = \frac{\text{Number of error bits per block}}{\text{Total number of bits per block}} \dots\dots\dots (3.1)$$

10k write/erase cycles are first applied. The measured program-disturb BER in 4Xnm NAND flash memory decreases as the “11” population increases (Fig. 12(a)). The measured program-disturb BER is decreased by 89%. Fig. 12(b) shows the measurement results in 3Xnm NAND flash memory. The program-disturb BER decreases due to the increase of the “11” population. The measured program-disturb BER is reduced by 73% (Fig. 12(b)). In case of 2Xnm NAND flash memory, if the population of “11” is increased, the program-disturb BER can be decreased (Fig 12(c)). The measured program-disturb BER is reduced by 71%. Therefore, the proposed asymmetric coding strategy which increases the “11” population works well for the program-disturb error.

IV. Proposed Asymmetric Coding Strategy for Data-Retention Error

A. Analyses of Error Rate of Each V_{TH} State for Data- Retention Error

Fig. 13 shows the state-error rate with the asymmetric coding for the data-retention error in 2Xnm NAND flash memory. If the “10” population is increased, “00” $\rightarrow$ “01” error and “10” $\rightarrow$ “00” error are lower than the state-error rate with the random pattern.

From the measurement results, if the “10” population increases, the state-error rate decreases. This is caused by the FG-FG coupling. The FG-FG coupling increases the V_{TH} state. On the other hand, the data-retention error decreases the V_{TH} state. The data-retention error is reduced by the FG-FG coupling. The FG-FG coupling induces negative effects on the program-disturb error whereas the FG-FG coupling works positively for the data-retention error. Therefore, when the “10” population increases, the state-error rate of the data-retention error is decreased. However, the data-retention BER with the increase of the “10” population is larger than the one with the random pattern (Fig. 14).

B. Data-Retention Error Reduction by Proposed Asymmetric-Coding Strategy

No data-retention error occurs in the “11” state since “11” is the lowest V_{TH} state (Fig. 15). The asymmetric coding maximizes the population of state “11”, so that the data-retention error is largely decreased.

Fig. 16 shows the data-retention error number per page. The code length of the proposed asymmetric coding is 2 bits. In lower page by using the proposed strategy, the number of data-retention error bit is reduced by 62%. On the other hand, the data-retention error number in the upper page is increased 14% by using the proposed strategy.

Fig. 17 shows the measured results of data retention error in 2Xnm, 3Xnm and 4Xnm NAND flash memories. 10k write/erase cycles are first applied before the asymmetric coding

measurement, and the retention time is 99 days. In case of the 4Xnm NAND flash memory, the data-retention BER decreases when the population of “11” increases (Fig. 17(a)). The measured data-retention BER with the proposed strategy is reduced by 70%. In addition, in 3Xnm NAND flash memory, if the population of “11” is increased, the data-retention BER becomes smaller (Fig. 17(b)). The measured data-retention BER is decreased by 52%. Fig. 17(c) shows the data-retention BER in 2Xnm NAND flash memory. If the “11” population is increased, the data-retention BER is decreased. The data-retention BER with the proposed strategy is reduced 17%. Thus, by using the proposed asymmetric coding strategy, the population of the lowest V_{TH} state is increased, so that the data-retention error is decreased.

V. CONCLUSION

Table 1 summarizes the improvement of the proposed strategy for program-disturb error and data-retention error. The proposed asymmetric coding strategy increases the lowest V_{TH} states. As a result, the V_{PGM} disturb and the FG-FG coupling is reduced. The program-disturb BERs in 2Xnm, 3Xnm and 4Xnm NAND flash memories decrease by 71%, 73% and 89%, respectively. For the data-retention error, the proposed asymmetric coding strategy increases the lowest V_{TH} state where no data-retention error occurs. The data-retention BERs in 2Xnm, 3Xnm and 4Xnm NAND flash memories decrease by 17%, 52% and 70%, respectively. Therefore, the proposed asymmetric coding strategy is effective for both the program-disturb error and the data-retention error.

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Figure 16: Bit-error number per page for data-retention error with random pattern and proposed asymmetric coding pattern.

Figure 17: Measured result for the data-retention error with the proposed asymmetric coding strategy in (a) 4Xnm, (b) 3Xnm and (c) 2Xnm NAND flash memories.

Figure 1

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Figure 6

Figure 7

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Figure 9

Figure 10

Figure 11

Figure 12

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Figure14

Figure 15

Figure 16

(a)

(b)

(c)

Figure 17

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Table 1: Summary of the proposed asymmetric coding strategy for program-disturb error and data-retention error.

	Memory cell size	Error pattern	V_{TH} distribution	Reliability
Random	4Xnm	—		—
	3Xnm			
	2Xnm			
Proposed coding	4Xnm	Program disturb error		<u>89% error reduction</u>
	3Xnm			<u>73% error reduction</u>
	2Xnm			<u>71% error reduction</u>
	4Xnm	Data retention error		<u>70% error reduction</u>
	3Xnm			<u>52% error reduction</u>
	2Xnm			<u>17% error reduction</u>

Table 1