Pareto analysis of critical challenges for emerging manufacturing technologies in silicon photovoltaics

KO Davis^{1,2,†}, RP Brooker^{1,2}, HP Seigneur^{1,2}, M Rodgers^{1,2}, AC Rudack^{1,3}, WV Schoenfeld^{1,2}

1. c-Si Division, U.S. Photovoltaic Manufacturing Consortium, 12354 Research Parkway – Suite 210, Orlando, FL 32826, USA
2. Florida Solar Energy Center, University of Central Florida, 1679 Clearlake Road, Cocoa, FL 32922, USA
3. SEMATECH, 257 Fuller Road, Albany, NY 12203 USA

† Corresponding author: Kris.Davis@uspvmc.org

Abstract: This work presents the results of a Pareto analysis of critical challenges for emerging manufacturing technologies in c-Si photovoltaics. By soliciting input from members of the PV R&D community, these challenges have been prioritized for six different sub-categories, the first three associated with *Processing Challenges* and the following three in the area of *Metrology Challenges*: (1) Feedstock, Crystallization and Wafering; (2) Cell Materials and Processing; (3) Module Integration; (4) Materials and Device Characterization; (5) Reliability and Durability (Measurements); and (6) Modeling and Simulation. Some sub-categories feature a large differential in scoring from the top challenge(s) to lower scored challenges (e.g. Module Integration, Modeling and Simulation), indicating topics of high interest. Other sub-categories feature a more evenly distributed level of prioritization (e.g. Cell Materials and Processing), indicating many high priority challenges within the same area. In total, 14 top critical challenges were identified for the six sub-categories, and a brief review for each of these is provided. As industry and academia seek R&D topics to help push for higher efficiencies and lower cost c-Si modules, this Pareto analysis can hopefully provide some objective insight into areas of high interest for the general PV community.

1. Introduction

In terms of market share, crystalline silicon (c-Si) solar cells and modules remain the dominant photovoltaic (PV) technology in terms of market share. Taking that into account, and the continued growth of the PV industry, there is significant interest in the prioritization of new manufacturing materials, processes, metrology techniques and modeling/simulation methods to increase efficiency and/or reduce cost. Most c-Si modules today feature Al back surface field (BSF) cells made from 180 μm *p*-type wafers, either monocrystalline Si (mono-Si) or multicrystalline Si (multi-Si), and laminated between glass and polymeric materials to form a rigid module with an Al-frame. From the production of the polysilicon used to make incoming wafers to the final assembly of modules, novel methods (i.e., emerging c-Si technologies) of improving performance and/or

reducing cost relative to the current technology have been proposed and, in some cases, implemented with varying levels of success.

The incredible cost reductions achieved over time for c-Si PV modules have been driven by both scale (i.e., increased capacity) and technology improvements. The focus of this paper is on the later, with an emphasis on what challenges may exist for emerging c-Si technologies seeking adoption by high-volume manufacturers. In 1999, Nijs *et al.* provided a review of manufacturing issues across the c-Si supply chain, describing the current state of wafer production and cell manufacturing, along with promising new wafer types and cell manufacturing processes yet to be adopted (Nijs *et al.*, 1999a). At the time, an important transition occurring in cell manufacturing was the adoption of plasma-enhanced chemical vapor deposition (PECVD) silicon nitride (SiN_x) as a passivation layer and anti-reflection coating (ARC) and the use of screen-printed Ag pastes with additives allowing manufacturers to fire through the ARC and contact the emitter. The near-term technologies discussed in this work include isotropic etching for multicrystalline Si (multi-Si) and selective emitter structures, which have both been rather successfully integrated by various manufacturers at high-volume.

In 2006, Swanson provided an explanation of the c-Si PV learning curve, giving a history perspective on module costs spanning a 30-year period, from the late 1970's to 2006 (Swanson, 2006). At this time, increased polysilicon costs due to a supply shortage was a large concern for c-Si manufacturers. Results of a 2002 survey of 23 experts at a National Renewable Energy Laboratory (NREL) workshop showed an expectation for drastic reductions in wafer thickness and module cost, along with significant efficiency reductions. The predicted wafer thickness reductions of the group ended up being too aggressive for mono-Si (120 μm by 2012), but rather close for multi-Si. Additionally, Swanson expressed an optimism that c-Si would remain the dominant conversion technology in the near-term (and likely longer), which has held true to this point in time. More recently, Aberle *et al.* provided a detailed and well-organized review of industrially relevant c-Si cell architectures and manufacturing processes, broken up by *p*-type architectures (standard and advanced) and *n*-type architectures (homojunctions and heterojunctions) (Aberle *et al.*, 2012). A road map for mono-Si PV authored by researchers from NREL Goodrich recently presented current and projected costs of various c-Si technologies across the supply chain (Goodrich *et al.*, 2013).

The U.S. Photovoltaic Manufacturing Consortium (PVMC) is an industry-led consortium that promotes cooperative R&D among industry, university and government partners (PVMC-Website, 2013). The two conversion technologies addressed by the PVMC include CIGS and c-Si. The c-Si activities are conducted at the University of Central Florida, where two previous Pareto exercises have been carried out for c-Si metrology (Davis *et al.*, 2012) and feedstock and wafering (Seigneur *et al.*, 2013). In this paper, the results of a targeted Pareto

analysis of critical challenges for emerging manufacturing technologies in c-Si PV are presented. The goal of this effort is to gain insight and prioritize the needs and challenges associated with the next generation of c-Si PV manufacturing process and metrology technologies across the entire supply chain (from polysilicon feedstock to completed modules). Input for this targeted Pareto exercise was gathered from 24 individuals representing 18 organizations at a PVMC workshop in Tampa, Florida (USA) on July 18, 2013. Most of the organizations represented in this Pareto analysis are from industry (13 people), however experts from universities (8 people), research institutes (2 people) and a national laboratory (1 person) were also included.

<i>Category or Sub-Category Name</i>	<i>Number of Challenges</i>
Processing	37
Feedstock, Crystallization and Wafering	11
Cell Materials and Processing	17
Module Integration	9
Metrology	27
Materials and Device Characterization	13
Reliability and Durability	8
Modeling and Simulation	6
--Total Number of Challenges--	64

Table 1. Breakdown of emerging c-Si technologies challenges by category and sub-category.

2. Pareto Methodology

For this Pareto, a total of 64 challenges were included, broken up into two primary categories, *Processing Challenges* and *Metrology Challenges*, each with their own sub-categories (Table 1). These challenges represent potential problems, barrier and areas of concern for future c-Si technologies and were created through a coordinated effort involving literature searches, consultation from industry and feedback from the Pareto participants. The prioritization ultimately ranks the extent to which the Pareto participants believe further R&D is needed. To rank this list of challenges, participants were asked to score each challenge between 0-5 (0 being the lowest priority and 5 the highest). Additionally, a finite number of points were provided for each sub-category (approximately proportional to the number of challenges within that sub-category), thereby forcing participants to only give high scores to those challenges deemed of high importance. Critical challenges for each sub-category were then defined as challenges receiving a score within one standard deviation (1σ) of the top score for that sub-category.

Participants were also instructed to keep in mind all of these challenges are within the context of emerging materials and devices (i.e. not standard technologies). For example, with the Reliability and Durability sub-category, the "Lack of physical understanding of failure modes" challenge refers to poorly understood mechanisms, such as how impurity precipitates in non-electronic

grade Si feedstocks might cause shunting problems, or how μ -cracks propagate in epitaxial wafers, in contrast to generally accepted reliability issues associated with standard 180 μm screen-printed Al back surface field (BSF) cells.

In the subsequent sections, the prioritized lists of challenges are provided. Additionally, a technical summary of each of the top critical challenges is also given to provide some context and background information of each of these important areas.

3. Results and Discussion

3.1 Processing Challenges

3.1.1 Feedstock, Crystallization and Wafering

The prioritized list of challenges for the Feedstock, Crystallization and Wafer sub-category is given in Figure 1. This section refers to the “front-end” processes required to create c-Si wafers. A brief summary of the top critical challenges ($1\sigma = 14.0$) is given as follows:

Reducing wafer sawing capability below 150 μm : Despite the reduction in the cost of polysilicon, material costs of silicon still represent approximately 50% of the total cost of a module in \$/Watt (Lacey, 2013). Therefore reducing wafer sawing capability well below 150 μm is in principle an attractive and viable solution to reducing cost in a cash-strapped industry focused on evolutionary rather than revolutionary changes. In fact, industry leader SunPower is believed to already use wafers on the order of 150 μm and below. In addition, sawing between 150 to 120 μm with equal kerf loss has been demonstrated on the industrial scale although with a lower throughput of 500 wafers per hour and 80 μm at the lab scale (Skumanich, 2009). The challenge in cutting such thin wafers reliably lies in the increased risk of the wafers breaking and the wire breaking (thinner wire is needed to reduce kerf loss and there is a lack of simple/affordable metrology to monitor the wire in real-time). Additionally, a reduced wafer thickness results in new technical challenges related to handling and processing (Popovich *et al.*, 2011; Schonfelder *et al.*, 2005).

Cost reduction and increased production capacity of *n*-type wafers: *P*-type Cz grown mono-Si and *p*-type multi-Si have been the workhorses of the PV industry representing more than 85% of commercial solar cells fabricated (Mihailetchi, 2006), while *n*-type mono-Si recently represented about 4% (Kopecek and Libal, 2012). Uniform boron doping during crystal growth is more easily achieved due to higher segregation coefficient of boron species with respect to phosphorus. Similarly, phosphorus doping during emitter formation on *p*-type substrates is easier/cheaper than boron doping during emitter formation on an *n*-type substrate. However, *p*-type substrates tend to suffer more from a performance (lower bulk lifetime, less immunity to metallic impurities), processing (less tolerant to high temperature) and reliability standpoint (light-induced degradation) (Mihailetchi, 2006). As a consequence, a shift to *n*-type substrates is anticipated in the future; the 2012 edition of the International Technology Roadmap for

Photovoltaics predicts up to 30% of market share by 2015. Continuous Cz (Ostrom *et al.*, 2013) and quasi-mono (Jouini *et al.*, 2013) are expected to be the vehicles that will enable the high-throughput production of *n*-type substrates for high-efficiency solar cells at a reasonable cost. Further cost reductions are in principle possible using UMG-Si feedstock if compensation engineering strategies are utilized (Forster *et al.*, 2013). From a cell fabrication perspective, boron implantation, BCl₃ or BBr₃ diffusion or atmospheric pressure chemical vapor deposition (APCVD) could be viable solutions for boron emitter formation (Benick *et al.*, 2012; Schiele *et al.*, 2013).

Improving the surface properties of diamond wire saw cuts: The surface morphology of diamond-sawn wafers, especially microcracks, greatly influences the mechanical strength of wafers (Chasiotis *et al.*, 2005; Wu *et al.*, 2012). Surfaces of slurry-cut wafers tend to have more pits, while diamond wire-cut wafers exhibit scratches and microcracks. The difference is due to the different cutting mechanisms. For slurry-based sawing, the accepted mechanism is the “rolling-indenting” model, where SiC particles roll across the surface and carve out sections of silicon. In contrast, diamond wire sawing generally tends to cut silicon wafers by “plastic ploughing” and “brittle chip-off” methods (Cai *et al.*, 2011). Microcracks tend to occur in the case of diamond wire sawing especially when sharp diamond grit are used resulting in a fracture rather ductile mode of cutting (Wu and Melkote, 2012). Nevertheless, diamond wire sawing can result in reduced saw damage compared to slurry based sawing (Bye *et al.*, 2011; Cai *et al.*, 2011). Furthermore, it must be noted that diamond wire sawing induces cracks along the wire direction along with phase change and stress (both tensile and compressive), which in turn reduces the failure strength of wafers along the wire direction compared to slurry-cut wafers (Bidiville *et al.*, 2010; Bidiville *et al.*, 2009). Equally critical are the edges; polishing or etching of the silicon ingot prior to wafering process can increase the strength of the wafers by 33% (Borrero-López *et al.*, 2009; Wasmer *et al.*, 2008). Related to improving the surface properties of diamond wire saw cuts is the fact that saw damage removal etch as well as surface texturing remains to be optimized (Meinel *et al.*, 2012). Future efforts for improving the wafer surface properties of diamond wire sawing are devoted to improved tension control and diamond coating of thin steel wires (Bye *et al.*, 2011).

ID	Challenge	Score
ETP-A6	Reducing wafer sawing capability below 150 μm	56
ETP-A4	Cost reduction and increased production capacity of <i>n</i> -type wafers	52
ETP-A7	Improve surface properties of diamond wire saw cuts	42
ETP-A11	Improved throughput and reduced defect density (e.g. seed layer) for epi-Si	39
ETP-A5	Improving mono-like ingots (e.g. dislocations, blocking mc-Si grain growth)	37
ETP-A2	Demonstration of higher purity UMG feedstock	31
ETP-A10	Reduced stress and impurities in direct wafers	30
ETP-A8	Lower cost and improved quality of implant/cleave cuts	23
ETP-A1	Scaling up low energy polysilicon EG production techniques	22
ETP-A9	Improve crack initiation/propagation and bow in wafers made by spalling	20
ETP-A3	Scaling up ingot production using novel dopant elements for Cz growth (e.g. Ga, In)	10

Figure 1. The prioritized list of challenges for the Feedstock, Crystallization and Wafer sub-category, with the top critical challenges highlighted in red.

3.1.2 Cell Materials and Processing

The Cell Materials and Processing sub-category refers to the conversion of wafers into cells, which includes (but isn't limited to) wet chemical processing, emitter formation, passivation and ARC deposition/growth and metallization. This sub-category features the most total challenges and the most top critical challenges with five falling within 1σ of the top challenge ($1\sigma = 11.3$). This indicates a broad range of challenges of high interest to the PV community.

Scaling up alternatives to standard texturing processing for improved light trapping: Improved light trapping is an area of high interest in c-Si PV, especially when one considers the desire to continually reduce wafer thickness below 180 μm to both reduce cost and potentially increase V_{OC} (Green, 1984). Since c-Si is an indirect bandgap semiconductor, it features a relatively low optical absorption coefficient. This means that, in addition to the need to reduce front surface reflectance (R_{fe}), a strategy to keep light within the cell is also important. The latter can be quantified by a light trapping constant (Z) that, when multiplied by the actual thickness of the wafer, results in the optical path length of the cell (McIntosh and Baker-Finch, 2012). There are many proven methods to both reduce R_{fe} and increase Z , with varying levels of effectiveness. To reduce R_{fe} in today's mainstream manufacturing, wet chemical texturing using either an alkaline or acid chemistry is used for monocrystalline and multicrystalline, respectively (Erk, 2010). There is room for improvement using this approach, and these wet processes might not be suitable for thin wafer formats (e.g. epitaxial c-Si wafers), hence the interest in alternatives. Due to parasitic absorption at the screen-printed Al contact layer at the rear side of the cell, standard Al-BSF cells

exhibit poor internal back reflectance, on the order of 60-70% (Basore, 1993; Davis *et al.*, 2013a; Gatz *et al.*, 2011; Kray *et al.*, 2008), thereby reducing Z .

Some alternative light trapping technologies that have been demonstrated on c-Si wafers and cells include the use of dry reactive ion etching (RIE) etching (Zaidi *et al.*, 2001), laser texturing (Sher *et al.*, 2011) and rear side dielectrics that can increase internal back reflectance above 95% (Davis *et al.*, 2013a; Kray *et al.*, 2008) and offer improved rear surface passivation, which is also critical for thin wafer formats (Willeke, 2002). More exotic light trapping schemes have been demonstrated on c-Si materials at lab-scale, including (but not limited to) plasmonic nanostructures (Munday and Atwater, 2010; Pillai *et al.*, 2007), photonic crystal designs (Bermel *et al.*, 2007; O'Brien *et al.*, 2008), moth eye structures (Yamada *et al.*, 2011), Si nanowires arrays (Dai *et al.*, 2010), graded-index coatings formed by oblique-angle deposition (Poxson *et al.*, 2011), rear side diffraction gratings (Barbé *et al.*, 2012; Peters *et al.*, 2012) and porous Si back reflectors (Bilyalov *et al.*, 2002; Duerinckx *et al.*, 2008). However, some of the methods requiring nanostructures employ fabrication methods unsuitable for the large area, low cost and high-throughput requirements associated with c-Si cell manufacturing. Therefore, this challenge represents the scaled-up manufacturing processes needed to realize these alternative light trapping designs.

Identification of appropriate substrates/carriers for thin wafer cell processing:

In order to significantly reduce material costs, thinner silicon wafers must be employed in the cells. However, multi-wire saw (MWS) techniques are not expected to fabricate wafers $<100\text{ }\mu\text{m}$, due to high sub-surface damage and kerf losses in excess of 50% (Beesley and Schonholzer, 2007; Dross *et al.*, 2012). Alternative approaches for thin-film silicon involve deposition techniques such as zone melting recrystallization, chemical vapor deposition, solution growth and solid phase crystallization (Nijs *et al.*, 1999b). For each of these techniques, a substrate is used to support the thin film. The selection of the substrate is based on the operating temperature of the thin film formation process. For example, zone melting recrystallization occurs at very high temperatures ($>1430^{\circ}\text{C}$), requiring the use of high temperature ceramics. Medium temperature ($700\text{--}1300^{\circ}\text{C}$) employ more economical substrates, while low temperature ($<700^{\circ}\text{C}$) use conventional glass. Restrictions on the substrates used for high temperature range include contamination of the silicon, and internal stresses during cool-down (from CTE mismatch). Low temperature thin film silicon processes are restricted in the crystallographic quality of the silicon, although processability is improved.

Microelectronics industry deals with very thin wafers by temporarily bonding them to a substrate, processing the wafers, then debonding the wafer (Tan and Reif, 2005).

Demonstration of high-throughput Cu plating technologies: Cu plating for metallization (instead of screen printing) will reduce shadow losses and series resistance, while improving contact with the emitter. However, in order to form Cu contacts with the cell surface, a metal seed layer must make contact with the emitter. This process step, known as pre-metallization (Aakella *et al.*, 2013), can be accomplished by various methods, such as laser ablation (Das *et al.*, 2011; Hernandez *et al.*, 2010), wet chemical/lithography (Michaelson *et al.*, 2012), and aerosol jet printing and firing (Glunz *et al.*, 2008). Laser ablation methods appear to be gaining in popularity, as this approach can be tailored so as to reduce emitter damage. However, it must be optimized for production-line speeds as well as solar cell efficiencies (Sugianto *et al.*, 2010).

Copper is a known contaminant in silicon solar cells, and must be prevented from diffusing into the cell. Common barriers to Cu migration include titanium (JaeSung *et al.*, 2002) and nickel, and these metals are frequently used as the pre-metallization step. Nickel silicide (NiSi) is gaining wider acceptance as the preferred copper barrier, although a cost-effective method for Ni application is still being sought (Jie *et al.*, 2010; Michaelson *et al.*, 2012). In order to form NiSi, the cell must be annealed at elevated temperatures (400-450°C), with annealing parameters influencing the final cell efficiency (Chaudhari and Solanki, 2010).

Cu plating is commonly achieved through light-induced plating methods (Glunz *et al.*, 2008), although the electrolyte solution must be optimized (Nguyen *et al.*, 2009). Notwithstanding the barriers to commercialization of this technology, production-line levels using laser-doped selective emitters (LDSE) solar cells have been achieved, with efficiencies of 19.3% (Hallam *et al.*, 2011). Other methods include electroless plating, although this step requires lithographic methods to define the metallization area, and may not be as amenable to production speeds.

Proven reliability/durability of Ag-free metallization: The leading candidate to replace Ag is Cu, for which the application, as was discussed above, is still being optimized. To date, there are very few detailed studies on the reliability and durability of c-Si solar cells featuring Cu metallization. However, Cu contamination of the Si, as well as ghost plating, are critical concerns that will influence the adoption of Ag-free metallization approaches. Copper contamination of silicon has been shown to significantly reduce carrier lifetimes (Davis *et al.*, 1980), and as such should be insulated from the silicon wafer (as described above). Therefore, the reliability of Ag-free metallization is related to the Cu-diffusion barrier's reliability. Additional modes of Cu-contamination include ghost-plating, where Cu is deposited outside the laser-opened regions in the ARC. This may be due to defects in the ARC, such as cracks and pinholes, where reduction of Cu-ions during plating occurs directly at the silicon surface (Braun *et al.*, 2011). Beyond the concerns over initial plating, the major concern for Cu reliability is the mechanical adhesion. Industrial experts wonder if good adhesion with Cu is possible at this time (Beaucarne *et al.*, 2012). The long-term

diffusion of Cu into silicon is viewed as a lesser concern, due to the possibility of incorporating successes from the microelectronics industry. However, it was also stated that the transition to Pb-free solder may be facilitated using Cu-plated contacts, since these tend to have improved solderability over Ag-fired contacts.

Low cost, high throughput alternatives to PECVD SiN_x and thermal oxides:

PECVD SiN_x is the primary material used today for emitter passivation in mainstream c-Si manufacturing. Thermal silicon oxide (SiO₂) films have also been used in the production of some high efficiency cells and have been used for a long time in lab-scale devices (Green *et al.*, 1999). The high temperature oxidation required for SiO₂ passivation is undesirable from a production and throughput perspective, due to process temperatures of $\approx 1000^\circ\text{C}$, and because it can degrade the bulk minority carrier lifetime of wafers (Aberle, 2000). The benefits of SiN_x over thermal SiO₂ include: (1) the ability to deposit the films at temperatures below 500°C ; (2) the positive fixed charge at the dielectric/semiconductor interface (providing field-effect passivation of *n*-type and *n*⁺ surfaces); (3) greater grain boundary passivation in multi-Si through incorporation of large amounts of hydrogen; and, (4) an adjustable refractive index that allows the film to also be used as a front side ARC (Aberle, 2000). Some shortcomings of PECVD SiN_x include the inability to effectively passivate *p*-type and *p*⁺ surfaces, since the positive Q_f causes parasitic shunting (Dauwe *et al.*, 2002), and the undesirable requirement of vacuum systems and batch processing (as opposed to in-line, non-vacuum processes).

Many low cost, high throughput alternatives to SiN_x and thermal SiO₂ have been studied. Intrinsic amorphous silicon (a-Si) deposited by PECVD is used in production today for high-efficiency heterojunction-based cells, providing cells with very high V_{OC} values, but a reduction in current due to parasitic absorption in this passivation layer is one downside (Mishima *et al.*, 2011). Aluminum oxide (AlO_x) is a material of high interest to the PV community right now, due to the ability to effectively passivate *p*-type and *p*⁺ surfaces (Dingemans and Kessels, 2012). While most of the studies to date have been performed using thermal and plasma-assisted atomic layer deposition (ALD), higher throughput methods have been developed recently, including spatial ALD (Poodt *et al.*, 2010; Vermang *et al.*, 2011), PECVD (Miyajima *et al.*, 2010; Saint-Cast *et al.*, 2012; Saint-Cast *et al.*, 2009) and APCVD (Black and McIntosh, 2012; Davis *et al.*, 2013b). Titanium oxide (TiO₂) has also been studied (Richards, 2003), since it can be synthesized and deposited very cheaply and has a tunable refractive index, like SiN_x. It was previously used by industry as an ARC layer, but the surface passivation provided is rather poor unless some type of intermediate SiO₂ interfacial layer is present (Richards *et al.*, 2002; Rohatgi *et al.*, 2000). Aluminum nitride is another material of interest due to similar optical properties of SiN_x, but a negative fixed charge (as with AlO_x), which allows it to be a potential front side passivation material for *n*-type wafers with *p*⁺ emitters (Krugel *et al.*, 2013).

ID	Challenge	Score
ETP-B1	Scaling up alternatives to standard texturing for improved light trapping	57
ETP-B13	Appropriate substrates/carriers for thin wafers during cell processing	53
ETP-B6	Demonstration of high-throughput Cu plating technologies	52
ETP-B7	Proven reliability/durability of Ag-free metallization	49
ETP-B3	Low cost, high throughput alternatives to PECVD SiN _x and thermal oxide	47
ETP-B5	Passivation of novel wafer formats	41
ETP-B9	Scaling up laser-based processing	41
ETP-B15	Development of new low-cost light trapping processes	37
ETP-B10	Low cost, high throughput patterning	34
ETP-B14	Gettering for low quality materials	33
ETP-B12	Scaling up of POCl ₃ alternatives	31
ETP-B2	Implementation of alternative light texturing processes onto thin wafer formats	31
ETP-B4	Conformal deposition onto light trapping nanostructures	28
ETP-B11	Demonstration of co-diffusion processes for simultaneous p^+ and n^+ doping	25
ETP-B16	Addressing edge effects and recombination	25
ETP-B8	Demonstration of low cost "seed-and-plate" technologies	23
ETP-B17	Al-based metallization (front and back) and robust soldering methods	22

Figure 2. The prioritized list of challenges for the Cell Materials and Processing sub-category, with the top critical challenges highlighted in red.

3.1.3 Module Integration

Module integration refers to the processing steps required to convert individual cells into complete modules. This typically involves the electrical interconnection of cells into strings (i.e. stringing and tabbing) and the lamination of these strings into an encapsulated module that can handle long-term operation outdoors. This sub-category featured the largest standard deviation ($1\sigma = 19.8$), resulting in two top critical challenges scoring significantly higher than the remaining challenges:

Breakage during lamination of thin wafers: Due to cost requirements, wafers for PV cells are becoming thinner. Creating thinner wafers leads to more breakage because thinner wafers are more brittle (Israil *et al.*, 2013; Little *et al.*, 2010b). Many processing steps, including lamination of cells into solar panels, induce stress on the wafers (Monastyrskiy *et al.*, 2008; Sander *et al.*, 2013). During lamination, stress results from the relatively large temperature difference of about 100 °C to 150 °C between the heating plate and the PV module upon insertion combined with the relatively low thermal conductivity of glass and the pressures that must be exerted on the module for lamination to occur (Lange *et al.*, 2011; Sander *et al.*, 2013). These stresses can result in warping or breaking of the wafers. Research in the optimization of the lamination process to result in minimal wafer breakage with a fast cycle time and a robust process window is needed (Lange *et al.*, 2011).

Breakage of thin wafers during stringing/tabbing: The requirement that PV manufacturing costs be reduced has resulted in a steady decrease in wafer thicknesses (Bragagnolo *et al.*, 2002; Gabor *et al.*, 2006). As solar cells become thinner, it becomes more difficult to interconnect them without breakage using standard soldering techniques (Gouttebroze *et al.*, 2013; Israil *et al.*, 2013; Little *et al.*, 2010b). High temperatures (250 °C to 400 °C) during soldering impart thermal and mechanical loads on the cells, which can result in warping and breakage of cells (Chen *et al.*, 2012; Gabor *et al.*, 2006). Besides being costly and wasteful, in-line breakage of wafers during stringing and tabbing also reduces equipment throughput due to downtime and the need to stop and clean out the machinery to remove the broken wafers (Hilmersson *et al.*, 2008). Processes, materials, and handling equipment must adapt to maintain acceptable mechanical yields and module reliability (Gabor *et al.*, 2006; Pingel *et al.*, 2009). Several researchers have tried addressing the issue of thin wafer breakage during stringing and tabbing by using a mechanical protective layer (Endroes *et al.*, 1997), optimizing the ribbon characteristics, (Gabor *et al.*, 2006; Pingel *et al.*, 2009) or using alternative interconnection techniques (Pingel *et al.*, 2009). However, these techniques have not been fully developed and have not been adopted in industry.

Figure 3. The prioritized list of challenges for the Module Integration sub-category, with the top critical challenges highlighted in red.

3.2 Metrology Challenges

3.2.1 Materials and Device Characterization

Two top critical challenges emerged within the Materials and Device Characterization sub-category ($1\sigma = 12.8$), out of a total of 13.

Measuring minority carrier lifetimes and extracting surface recombination velocities on novel materials and wafer formats: The effective minority carrier lifetime (τ_{eff}) of a cell is dependent on recombination processes occurring within the bulk of the material and at the surface of the cell. One of the challenges in extracting the surface recombination velocity (S_{eff}) for a surface is trying to decouple the bulk (τ_{bulk}) and surface ($\tau_{surface}$) from τ_{eff} . Traditionally, the extraction

of S_{eff} has been performed by depositing passivation layers on both sides of wafers with a very long τ_{bulk} (e.g. high-resistivity wafers, float-zone wafers) and then measuring τ_{eff} by photoconductance decay (Sinton and Cuevas, 1996) or some other method. By assuming $\tau_{bulk} \gg \tau_{surface}$, the following equation can be used to approximate the maximum S_{eff} (Sproul, 1994):

$$S_{eff} = \frac{W}{2\tau_{eff}}$$

where W is the wafer thickness. However, in the case of many emerging c-Si technologies, it might not be possible to make a test structure like this. Consider novel surface textures, feedstock materials with relatively low τ_{bulk} and epitaxial c-Si wafers connected to carrier substrates. Both the ability to accurately measure τ_{eff} on these novel samples and developing improved methods of extracting S_{eff} from τ_{eff} are therefore of interest to the PV community.

Cost effective methods of characterizing impurities in a manufacturing setting: Different types of impurities have varying effects on PV cells. Metallic and ionic impurities (1) decrease the minority carrier diffusion length, resulting in loss of cell performance and (2) corrosively etch critical surfaces, leading to over etching, which can result in pre-breakdown (Fenning *et al.*, 2013; Yoon *et al.*, 2012; Zuschlag *et al.*, 2010). Characterization of materials and process parameters during manufacturing is extremely important for detecting impurities early in the process and ensuring the products will be within specifications. Current impurity characterization methods, such as x-ray photoelectron spectroscopy, x-ray or electron beam-stimulated Auger emission, or x-ray fluorescence spectroscopy, tend to be off line, destructive, and/or cost prohibitive (Fenner *et al.*, 1989; Zuschlag *et al.*, 2010). A key desirable capability in solar cells is cost-effective, in-situ monitoring of impurities during processing. Inline, non-destructive measurements are preferred to reduce wasting of time and resources (Little *et al.*, 2010b).

ID	Challenge	Score
ETM-A3	Measuring minority carrier lifetimes and SRV on novel materials and wafer formats	66
ETM-A2	Cost effective methods of characterizing impurities in a manufacturing setting	55
ETM-A6	Correlation of stress/strain to cracks	49
ETM-A12	Standardized test for evaluating mechanical integrity of wafers	49
ETM-A7	Identification of μ -cracks	48
ETM-A10	Implementation of new off-line techniques to in-line	42
ETM-A11	In-line characterization for edge isolation	40
ETM-A4	Quantifying light trapping enhancements incorporating front and rear-side optics	40
ETM-A9	Measuring EQE/IQE and light I-V characteristics of novel sample types	39
ETM-A13	Application of thermal and mechanical test methods to thin wafers	34
ETM-A5	Measuring thickness and optical parameters on atypical surface textures	31
ETM-A1	Chemical mapping with high-spatial resolution	27
ETM-A8	Improved methods of characterizing diode properties for novel materials and wafers	16

Figure 4. List of prioritized Metrology Challenges, sub-category Materials and Device Characterization

3.2.2 Reliability and Durability

The technology associated with current c-Si PV modules has a long proven track record as a reliable producer of energy. The emergence of new materials, processing techniques or device concepts introduces potential uncertainty in the reliability and durability of a given c-Si module. Metrology related to the reliability and durability of these emerging c-Si technologies refers to the measurements and test methods used to evaluate whether or not the new technology has a negative impact of the long-term performance. This sub-category features the smallest standard deviation ($1\sigma = 10.4$), resulting in only one top critical challenge. Similar to the Cell Materials and Processing sub-category, this small 1σ value indicates a broad interest in many challenges, as opposed to the clear dominant prioritization of just a few.

Early screening methods to identify potential shortcomings of new technologies: Demonstrating reliability and durability is especially important for emerging technologies that do not have as many years of demonstrated field performance. Without a sufficient complement of in-line tools, it is difficult to detect, early in the manufacturing process, the wide variety of defects that can degrade the quality and performance of the finished product. Testing equipment that can detect and potentially correct defects in real time would increase throughput and yield and mitigate reliability concerns (Little *et al.*, 2010a).

In addition to the equipment required for screening, developing the appropriate accelerated stress tests to identify failure is needed. Current QA testing is

insufficient for long-term durability guarantees, and there is a need to develop tests that can accurately predict the lifetime of components in fielded modules, but to conduct the test over a short period of time. The International PV QA Task Force was developed to address this need, and is currently investigating accelerated stress testing (Wohlgemuth, 2013).

ID	Challenge	Score
ETM-B7	Early screening methods to identify potential shortcomings of new technologies	65
ETM-B2	Lack of understanding of failure modes	53
ETM-B1	Need for techniques to perform Root Cause analysis of failures in novel samples	48
ETM-B6	Need to create or modify existing accelerated aging tests on novel samples	47
ETM-B5	Lack of physical understanding of degradation mechanisms	47
ETM-B8	Understanding how and if existing test methods can be applied to novel samples	37
ETM-B4	Need for standardized test methods to quantify degradation in novel sample types	35
ETM-B3	Correlation of material quality and degradation	34

Figure 5. List of prioritized **Metrology Challenges**, sub-category Reliability and Durability

3.2.3 Modeling and Simulation

Modeling and simulation is a critical element of pushing technology forward. In this sub-category, one challenge clearly emerged as the top critical challenge with a differential of a 40% between it and the second rated challenge. The relatively high standard deviation of this group ($1\sigma = 18.9$) is driven primarily by the high score for the top challenge.

Integration of metrology data into modeling tools (and vice versa) to allow for better process control: Developing advanced PV cells involves expensive research and experimentation. Improved cycles of learning are achieved by utilizing properly designed modeling and simulation tools that allow for the direct manipulation of materials, dimensions, doping levels, structures, optical properties and back-surface fields/reflectors (Michael *et al.*, 2005). Modeling and simulation tools need to be verified and refined by experimental results, including novel metrology techniques that are required for advanced cell architectures. Ideally, in-line or *in situ* metrology can be utilized to provide real-time feedback when properly implemented in advanced cell manufacturing as process control. This integration of metrology data and modeling tools remains a challenge.

(c)

ID	Challenge	Score
ETM-C4	Integration of metrology data into modeling tools (and vice versa) and process control	87
ETM-C2	Compatibility of existing models with novel materials and advanced cell architectures	52
ETM-C6	Lack of open data sharing and easy to access databases for experimental validation	49
ETM-C5	Lack of sufficient experimental validation for existing models	43
ETM-C3	Quality of free and/or open source models	38
ETM-C1	Software license cost	35

Figure 6. List of prioritized *Metrology Challenges*, sub-category Modeling and Simulation

4. Conclusions

In conclusion, this work presents the results of a Pareto analysis of critical challenges for emerging manufacturing technologies in c-Si photovoltaics. By soliciting input from members of the PV R&D community, these challenges have been prioritized for six different sub-categories, the first three associated with *Processing Challenges* and the following three in the area of *Metrology Challenges*: (1) Feedstock, Crystallization and Wafering; (2) Cell Materials and Processing; (3) Module Integration; (4) Materials and Device Characterization; (5) Reliability and Durability (Measurements); and (6) Modeling and Simulation. Some sub-categories feature a large differential in scoring from the top challenge(s) to lower scored challenges (e.g. Module Integration, Modeling and Simulation), indicating topics of high interest. Other sub-categories feature a more evenly distributed level of prioritization (e.g. Cell Materials and Processing), indicating many high priority challenges within the same area. In total, 14 top critical challenges were identified for the six sub-categories, and a brief review for each of these is provided. As industry and academia seek R&D topics to help push for higher efficiencies and lower cost c-Si modules, this Pareto analysis can hopefully provide some objective insight into areas of high interest for the general PV community.

Acknowledgements

This material is based upon work supported by the Department of Energy's Office of Energy Efficiency and Renewable Energy, in the Solar Energy Technologies Program, under Award Number DE-EE0004947. This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not

necessarily state or reflect those of the United States Government or any agency thereof. All service marks and trademarks of the U.S. Photovoltaic Manufacturing Consortium (PVMC), the SUNY College of Nanoscale Science & Engineering (CNSE), SEMATECH, and the University of Central Florida (UCF) are the property of their respective owners.

References

- Aakella, P.S., Saravanan, S., Joshi, S.S., Solanki, C.S., 2013. Pre-metallization processes for c-Si solar cells, *Sol Energy*, 97, 388-397.
- Aberle, A.G., 2000. Surface Passivation of Crystalline Silicon Solar Cells: A Review, *Progress in Photovoltaics: Research and Applications*, 8, 473-487.
- Aberle, A.G., Boreland, M.B., Hoex, B., Mueller, T., 2012. Industrial Silicon Wafer Solar Cells – Status and Trends, *Green*, 2.
- Barbé, J., Thomson, A.F., Wang, E.-C., McIntosh, K., Catchpole, K., 2012. Nanoimprinted TiO₂ sol-gel passivating diffraction gratings for solar cell applications, *Progress in Photovoltaics: Research and Applications*, 20, 143-148.
- Basore, P.A., 1993. In: *Proceedings of the 23rd IEEE Photovoltaic Specialists Conference*, Louisville, KY, pp. 147-152.
- Beaucarne, G., Schubert, G., Hoornstra, J., Horzel, J., Glunz, S.W., 2012. Summary of the Third Workshop on Metallization for Crystalline Silicon Solar Cells, *Energy Procedia*, 21, 2-13.
- Beesley, J.G., Schonholzer, U., 2007. In: *Proceedings of the 22nd European Photovoltaic Solar Energy Conference*, Milan, Italy, pp.
- Benick, J., Muller, R., Bateman, N., Hermle, M., 2012. In: *Proceedings of the 27th EU PVSEC Conference*, Frankfurt, Germany, pp.
- Bermel, P., Luo, C., Zeng, L., Kimerling, L.C., Joannopoulos, J.D., 2007. Improving thin-film crystalline silicon solar cell efficiencies with photonic crystals, *Opt. Express*, 15, 16986-17000.
- Bidiville, A., Heiber, J., Wasmer, K., Habegger, S., Assi, F., 2010. In: *Proceedings of the 25th European Photovoltaic Solar Energy Conference and Exhibition / 5th World Conference on Photovoltaic Energy Conversion Valencia*, Spain, pp.
- Bidiville, A., Wasmer, K., Kraft, R., Ballif, C., 2009. In: *Proceedings of the 24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, pp.
- Bilyalov, R., Solanki, C.S., Poortmans, J., Richard, O., Bender, H., Kummer, M., von Känel, H., 2002. Crystalline silicon thin films with porous Si backside reflector, *Thin Solid Films*, 403-404, 170-174.
- Black, L.E., McIntosh, K.R., 2012. Surface passivation of c-Si by atmospheric pressure chemical vapor deposition of Al₂O₃, *Applied Physics Letters*, 100, 202107-202101-202107-202105.
- Borrero-López, O., Vodenitcharova, T., Hoffman, M., Leo, A.J., 2009. Fracture Strength of Polycrystalline Silicon Wafers for the Photovoltaic Industry, *Journal of the American Ceramic Society*, 92, 2713-2717.

Bragagnolo, J.A., Akita, J., Sato, H., Chikaki, Y., Hashimoto, T., Ito, M., Sugiyama, I., Shea, S.P., 2002. In: Proceedings of the Photovoltaic Specialists Conference, 2002. Conference Record of the Twenty-Ninth IEEE, pp. 383-386.

Braun, S., Zuschlag, A., Raabe, B., Hahn, G., 2011. The Origin of Background Plating, *Energy Procedia*, 8, 565-570.

Bye, J.-I., Norheim, L., Holme, B., Nielsen, O., Steinsvik, S., Jensen, S.A., Fragiaco, G., Lombardi, I., 2011. In: Proceedings of the 26th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany, pp.

Cai, E., Tang, B., Fahrner, W.R., Zhou, L., 2011. In: Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, pp.

Chasiotis, I., Cho, S.W., Jonnalagadda, K., 2005. Fracture Toughness and Subcritical Crack Growth in Polycrystalline Silicon, *Journal of Applied Mechanics*, 73, 714-722.

Chaudhari, V.A., Solanki, C.S., 2010. In: Proceedings of the Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE, pp. 001322-001324.

Chen, Y.M., Chiu, Y.-P., Wu, H.-w., 2012. Improved Testing of Soldered Interconnects Quality on Silicon Solar Cell, *Global Perspectives on Engineering Management* 1, 51-58.

Dai, Y.-A., Chang, H.-C., Lai, K.-Y., Lin, C.-A., Chung, R.-J., Lin, G.-R., He, J.-H., 2010. Subwavelength Si nanowire arrays for self-cleaning antireflection coatings, *Journal of Materials Chemistry*, 20, 10924-10930.

Das, J., Tous, L., Hernandez, J.L., Jaffrennou, P., Ngamo, M., John, J., Posthuma, N.E., Baert, K., Poortmans, J., 2011. In: Proceedings of the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, pp.

Dauwe, S., Mittelstädt, L., Metz, A., Hezel, R., 2002. Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells, *Progress in Photovoltaics: Research and Applications*, 10, 271-278.

Davis, J.R., Jr., Rohatgi, A., Hopkins, R.H., Blais, P.D., Rai-Choudhury, P., McCormick, J.R., Mollenkopf, H.C., 1980. Impurities in silicon solar cells, *Electron Devices, IEEE Transactions on*, 27, 677-687.

Davis, K.O., Jiang, K., Demberger, C., Zunft, H., Haverkamp, H., Habermann, D., Schoenfeld, W.V., 2013a. Investigation of the Internal Back Reflectance of Rear-Side Dielectric Stacks for c-Si Solar Cells, *IEEE Journal of Photovoltaics*, 3, 641-648.

Davis, K.O., Jiang, K., Wilson, M., Demberger, C., Zunft, H., Haverkamp, H., Habermann, D., Schoenfeld, W.V., 2013b. Influence of precursor gas ratio and firing on silicon surface passivation by APCVD aluminium oxide, *physica status solidi (RRL) – Rapid Research Letters*, 7, 942-945.

Davis, K.O., Seigneur, H.P., Rudack, A.C., Schoenfeld, W.V., PVMC Tackles c-Si Metrology Challenges, in: *Future Photovoltaics*, 2012.

Dingemans, G., Kessels, W.M.M., 2012. Status and prospects of Al₂O₃-based surface passivation schemes for silicon solar cells, *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films*, 30, 040802-040801-040802-040827.

Dross, F., Baert, K., Bearda, T., Deckers, J., Depauw, V., El Daif, O., Gordon, I., Gougam, A., Govaerts, J., Granata, S., Labie, R., Loozen, X., Martini, R.,

Masolin, A., O'Sullivan, B., Qiu, Y., Vaes, J., Van Gestel, D., Van Hoeymissen, J., Vanleenhove, A., Van Nieuwenhuysen, K., Venkatachalam, S., Meuris, M., Poortmans, J., 2012. Crystalline thin-foil silicon solar cells: where crystalline quality meets thin-film processing, *Progress in Photovoltaics: Research and Applications*, 20, 770-784.

Duerinckx, F., Kuzma-Filipek, I., Van Nieuwenhuysen, K., Beaucarne, G., Poortmans, J., 2008. Simulation and implementation of a porous silicon reflector for epitaxial silicon solar cells, *Progress in Photovoltaics: Research and Applications*, 16, 399-407.

Endroes, A., Eisenrith, K.-H., Martinelli, G., Method for processing thin wafers and solar cells of crystalline silicon, in, Siemens Aktiengesellschaft. Munich. Germany, United States, 1997.

Erk, H.F., 2010. Wet Etching Technology for Semiconductor and Solar Silicon Manufacturing: Part 2-Process, Equipment and Implementation, *ECS Transactions*, 27, 1073-1080.

Fenner, D.B., Biegelsen, D.K., Bringans, R.D., 1989. Silicon surface passivation by hydrogen termination: A comparative study of preparation methods, *Journal of Applied Physics*, 66, 419-424.

Fenning, D.P., Zuschlag, A.S., Bertoni, M.I., Lai, B., Hahn, G., Buonassisi, T., 2013. Improved iron gettering of contaminated multicrystalline silicon by high-temperature phosphorus diffusion, *Journal of Applied Physics*, 113.

Forster, M., Dehestru, B., Thomas, A., Fourmond, E., Einhaus, R., Cuevas, A., Lemiti, M., 2013. Compensation engineering for uniform n-type silicon ingots, *Solar Energy Materials and Solar Cells*, 111, 146-152.

Gabor, A.M., Ralli, M., Montminy, S., Alegria, L., Bordonaro, C., Woods, J., Felton, L., Davis, M., Atchley, B., Williams, T., 2006. In: *Proceedings of the Proceedings of the 21st European Photovoltaic Solar Energy Conference*, pp. 2042-2047.

Gatz, S., Hannebauer, H., Hesse, R., Werner, F., Schmidt, A., Dullweber, T., Schmidt, J., Bothe, K., Brendel, R., 2011. 19.4%-efficient large-area fully screen-printed silicon solar cells, *physica status solidi (RRL) - Rapid Research Letters*, 5, 147-149.

Glunz, S.W., Aleman, M., Bartsch, J., Bay, N., Bayer, K., Bergander, R., Filipovic, A., Greil, S., Grohe, A., Ho, x, rteis, M., Knorz, A., Menko, M., Mette, A., Pysch, D., Radtke, V., Richter, P., Rudolph, D., Rublack, T., Schetter, C., Schmidt, D., Schultz, O., Woehl, R., 2008. In: *Proceedings of the Photovoltaic Specialists Conference, 2008. PVSC '08. 33rd IEEE*, pp. 1-4.

Goodrich, A., Hacke, P., Wang, Q., Sopori, B., Margolis, R., James, T.L., Woodhouse, M., 2013. A wafer-based monocrystalline silicon photovoltaics road map: Utilizing known technology improvement opportunities for further reductions in manufacturing costs, *Solar Energy Materials and Solar Cells*, 114, 110-135.

Gouttebroze, S., Lange, H.I., Ma, X., Glockner, R., Emamifard, B., Syvertsen, M., Vardavoulis, M., Ulyashin, A., 2013. Comparative analysis of mechanical properties of Si substrates processed by different routes, *Phys. Status Solidi A-Appl. Mat.*, 210, 777-784.

Green, M.A., 1984. Limits on the open-circuit voltage and efficiency of silicon solar cells imposed by intrinsic Auger processes, *IEEE Transactions on Electron Devices*, 31, 671-678.

Green, M.A., Zhao, J., Wang, A., Wenham, S.R., 1999. Very high efficiency silicon solar cells-science and technology, *IEEE Transactions on Electron Devices*, 46, 1940-1947.

Hallam, B., Wenham, S., Chong, C.M., Sugianto, A., Ly, M., Edwards, M., Jordan, D., Fath, P., 2011. In: *Proceedings of the Photovoltaic Specialists Conference (PVSC)*, 2011 37th IEEE, pp. 000047-000047.

Hernandez, J.L., Allebe, C., Tous, L., John, J., Poortmans, J., 2010. In: *Proceedings of the Photovoltaic Specialists Conference (PVSC)*, 2010 35th IEEE, pp. 003158-003162.

Hilmersson, C., Hess, D.P., Dallas, W., Ostapenko, S., 2008. Crack detection in single-crystalline silicon wafers using impact testing, *Appl. Acoust.*, 69, 755-760.

Israil, M., Anwar, S.A., Abdullah, M.Z., 2013. Automatic detection of micro-crack in solar wafers and cells: a review, *Trans. Inst. Meas. Control*, 35, 606-618.

JaeSung, Y., Jinmo, K., Kim, D., Pak, J.J., Choon-Sik, K., 2002. In: *Proceedings of the Photovoltaic Specialists Conference*, 2002. Conference Record of the Twenty-Ninth IEEE, pp. 277-280.

Jie, G., Ming, L., Dali, M., 2010. In: *Proceedings of the Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, 2010 11th International Conference on, pp. 310-313.

Jouini, A., Fortin, G., Marie, B., Enjalbert, N., Monna, R., 2013. In: *Proceedings of the 28th EU PVSEC*, Paris, France, pp.

Kopecek, R., Libal, J., Switch from p to n in: *pv magazine*, http://www.pv-magazine.com/archive/articles/beitrag/switch-from-p-to-n-_100007072/86/?tx_ttnews%5BbackCat%5D=201&cHash=d448ac5cc4ed9a022683711523e56d9d-axzz2gO7qCJkr, 2012.

Kray, D., Hermle, M., Glunz, S.W., 2008. Theory and experiments on the back side reflectance of silicon wafer solar cells, *Progress in Photovoltaics: Research and Applications*, 16, 1-15.

Krugel, G., Sharma, A., Wolke, W., Rentsch, J., Preu, R., 2013. Study of hydrogenated AlN as an anti-reflective coating and for the effective surface passivation of silicon, *physica status solidi (RRL) – Rapid Research Letters*, 7, 457-460.

Lacey, S., Top Chinese Manufacturers Will Produce Solar Panels for 42 Cents per Watt in 2015, in: *Greentechsolar*, <http://www.greentechmedia.com/articles/read/top-chinese-manufacturers-will-produce-solar-panels-for-42-cents-a-wat>, 2013.

Lange, R.F.M., Luo, Y., Polo, R., Zahnd, J., 2011. The lamination of (multi)crystalline and thin film based photovoltaic modules, *Progress in Photovoltaics: Research and Applications*, 19, 127-133.

Little, R.G., Collins, R., Anderson, T., Buller, B., Dennler, G., Gloeckler, M., Karam, N.H., Kurtz, S., Olson, D., Surek, T., Wohlgemuth, J., 2010a. In: *Proceedings of the Grand Challenges for Advanced Photovoltaic Technologies and Measurements Workshop*, Denver, Colorado, pp.

Little, R.G., Collins, R., Anderson, T., Buller, B., Dennler, G., Gloeckler, M., Karam, N.H., Kurtz, S., Olson, D., Surek, T., Wohlgemuth, J., Workshop Report: Grand Challenges for Advanced Photovoltaic Technologies and Measurements, May 11–12, 2010, Denver, Colorado, in, National Institute of Standards and Technology, 2010b, pp. 81.

McIntosh, K.R., Baker-Finch, S.C., 2012. In: Proceedings of the 38th IEEE Photovoltaic Specialists Conference, Austin, TX, pp. 265-271.

Meinel, B., Koschwitz, T., Acker, J., 2012. Textural development of SiC and diamond wire sawed sc-silicon wafer, *Energy Procedia*, 27, 330-336.

Michael, S., Bates, A.D., Green, M.S., 2005. In: Proceedings of the 21st IEEE Photovoltaic Specialists Conference, Lake Buena Vista, FL, pp. 719-721.

Michaelson, L., Munoz, K., Wang, J.C., Xi, Y.A., Tyson, T., Gallegos, A., 2012. In: Proceedings of the Photovoltaic Specialists Conference (PVSC), 2012 38th IEEE, pp. 002208-002212.

Mihailetchi, V., N-type silicon solar cell with Al back junction: results and modeling, in: 16th Crystalline Silicon Workshop, Colorado, US, 2006.

Mishima, T., Taguchi, M., Sakata, H., Maruyama, E., 2011. Development status of high-efficiency HIT solar cells, *Solar Energy Materials and Solar Cells*, 95, 18-21.

Miyajima, S., Irikawa, J., Yamada, A., Konagai, M., 2010. High Quality Aluminum Oxide Passivation Layer for Crystalline Silicon Solar Cells Deposited by Parallel-Plate Plasma-Enhanced Chemical Vapor Deposition, *Applied Physics Express*, 3, 012301.

Monastyrskyi, A., Ostapenko, S., Polupan, O., Maeckel, H., Vazquez, M., 2008. In: Proceedings of the Photovoltaic Specialists Conference, 2008. PVSC '08. 33rd IEEE, pp. 1-6.

Munday, J.N., Atwater, H.A., 2010. Large Integrated Absorption Enhancement in Plasmonic Solar Cells by Combining Metallic Gratings and Antireflection Coatings, *Nano Letters*, 11, 2195-2201.

Nguyen, A., Fioramonti, A., Morrissey, D., Efstathiadis, H., Zhao, Z., Haldar, P., 2009. In: Proceedings of the Photovoltaic Specialists Conference (PVSC), 2009 34th IEEE, pp. 000312-000315.

Nijs, J.F., Szlufcik, J., Poortmans, J., Sivoththaman, S., Mertens, R.P., 1999a. Advanced manufacturing concepts for crystalline silicon solar cells, *IEEE Transactions on Electron Devices*, 46, 1948-1969.

Nijs, J.F., Szlufcik, J., Poortmans, J., Sivoththaman, S., Mertens, R.P., 1999b. Advanced manufacturing concepts for crystalline silicon solar cells, *Electron Devices, IEEE Transactions on*, 46, 1948-1969.

O'Brien, P.G., Kherani, N.P., Chutinan, A., Ozin, G.A., John, S., Zukotynski, S., 2008. Silicon Photovoltaics Using Conducting Photonic Crystal Back-Reflectors, *Advanced Materials*, 20, 1577-1582.

Ostrom, N.P., Richardson, C., Ok, Y.-W., Tao, Y., Upadhyaya, A.D., Rohatgi, A., 2013. In: Proceedings of the 28th EU PVSEC, Paris, France, pp.

Peters, M., Rüdiger, M., Hauser, H., Hermle, M., Bläsi, B., 2012. Diffractive gratings for crystalline silicon solar cells—optimum parameters and loss

mechanisms, *Progress in Photovoltaics: Research and Applications*, 20, 862-873.

Pillai, S., Catchpole, K.R., Trupke, T., Green, M.A., 2007. Surface plasmon enhanced silicon solar cells, *Journal of Applied Physics*, 101, 093105.

Pingel, S., Zemen, Y., Frank, O., Geipel, T., Berghold, J., 2009. Mechanical stability of solar cells within solar panels, *Proc. of 24th EUPVSEC*, 3459-3464.

Poodt, P., Lankhorst, A., Roozeboom, F., Spee, K., Maas, D., Vermeer, A., 2010. High-speed spatial atomic-layer deposition of aluminum oxide layers for solar cell passivation, *Advanced Materials*, 22, 3564-3567.

Popovich, V.A., Yunus, A., Janssen, M., Richardson, I.M., Bennett, I.J., 2011. Effect of silicon solar cell processing parameters and crystallinity on mechanical strength, *Solar Energy Materials and Solar Cells*, 95, 97-100.

Poxson, D.J., Kuo, M.-L., Mont, F.W., Kim, Y.S., Yan, X., Welser, R.E., Sood, A.K., Cho, J., Lin, S.-Y., Schubert, E.F., 2011. High-performance antireflection coatings utilizing nanoporous layers, *MRS Bulletin*, 36, 434-438.

PVMC Website, <http://uspvmc.org>

Richards, B.S., 2003. Single-material TiO₂ double-layer antireflection coatings, *Solar Energy Materials and Solar Cells*, 79, 369-390.

Richards, B.S., Cotter, J.E., Honsberg, C.B., 2002. Enhancing the surface passivation of TiO₂ coated silicon wafers, *Applied Physics Letters*, 80, 1123.

Rohatgi, A., Doshi, P., Moschner, J., Lauinger, T., Aberle, A.G., Ruby, D.S., 2000. Comprehensive study of rapid, low-cost silicon surface passivation technologies, *IEEE Transactions on Electron Devices*, 47, 987-993.

Saint-Cast, P., Kania, D., Heller, R., Kuehnhold, S., Hofmann, M., Rentsch, J., Preu, R., 2012. High-temperature stability of c-Si surface passivation by thick PECVD Al₂O₃ with and without hydrogenated capping layers, *Applied Surface Science*.

Saint-Cast, P., Kania, D., Hofmann, M., Benick, J., Rentsch, J., Preu, R., 2009. Very low surface recombination velocity on p-type c-Si by high-rate plasma-deposited aluminum oxide, *Applied Physics Letters*, 95, 151502.

Sander, M., Dietrich, S., Pander, M., Ebert, M., Bagdahn, J., 2013. Systematic investigation of cracks in encapsulated solar cells after mechanical loading, *Solar Energy Materials and Solar Cells*, 111, 82-89.

Schiele, Y., Fahr, S., Joos, S., Hahn, G., Terheiden, B., 2013. In: *Proceedings of the 28th EU PVSEC*, Paris, France, pp.

Schonfelder, S., Bagdahn, J., Ebert, M., Petzold, M., Bock, K., Landesberger, C., 2005. In: *Proceedings of the Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems*, 2005. EuroSimE 2005. *Proceedings of the 6th International Conference on*, pp. 105-111.

Seigneur, H.P., Davis, K.O., Rudack, A.C., Schoenfeld, W.V., PVMC Tackles c-Si Feedstock and Wafering Challenges, in: *Future Photovoltaics*, 2013.

Sher, M.-J., Winkler, M.T., Mazur, E., 2011. Pulsed-laser hyperdoping and surface texturing for photovoltaics, *MRS Bulletin*, 36, 439-445.

Sinton, R.A., Cuevas, A., 1996. Contactless determination of current-voltage characteristics and minority carrier lifetimes in semiconductors from quasi-steady-state photoconductance data, *Applied Physics Letters*, 69, 2510-2512.

Skumanich, A., The art of wafer cutting in the PV industry, in: Renewable Energy World, http://www.renewableenergyworld.com/rea/news/article/2009/06/the-art_of_wafer_cutting, 2009.

Sproul, A.B., 1994. Dimensionless solution of the equation describing the effect of surface recombination on carrier decay in semiconductors, *Journal of Applied Physics*, 76, 2851.

Sugianto, A., Bovatsek, J., Wenham, S., Tjahjono, B., Guangqi, X., Yu, Y., Hallam, B., Xue, B., Kuepper, N., Chong, C.M., Patel, R., 2010. In: *Proceedings of the Photovoltaic Specialists Conference (PVSC)*, 2010 35th IEEE, pp. 000689-000694.

Swanson, R.M., 2006. A vision for crystalline silicon photovoltaics, *Progress in Photovoltaics: Research and Applications*, 14, 443-453.

Tan, C.S., Reif, R., 2005. Microelectronics Thin Film Handling and Transfer Using Low-Temperature Wafer Bonding, *Electrochem. Solid-State Lett.*, 8, G362-G366.

Vermang, B., Rothschild, A., Racz, A., John, J., Poortmans, J., Mertens, R., Poodt, P., Tiba, V., Roozeboom, F., 2011. Spatially separated atomic layer deposition of Al_2O_3 , a new option for high-throughput Si solar cell passivation, *Progress in Photovoltaics: Research and Applications*, 19, 733-739.

Wasmer, K., Bidiville, A., Jeanneret, F., Michler, J., Ballif, C., Van-der-Meer, M., Nasch, P.M., Effects of edge defects induced by multi-wire sawing on the wafer strength, in: *23rd European Photovoltaic Solar Energy Conference*, Valencia, 2008, pp. 1305-1310.

Willeke, G.P., 2002. Thin crystalline silicon solar cells, *Solar Energy Materials & Solar Cells*, 72, 191-200.

Wohlgemuth, J., 2013. In: *Proceedings of the Photovoltaic Module Reliability Workshop 2013*, Golden, Colorado, pp.

Wu, H., Melkote, S.N., 2012. Study of Ductile-to-Brittle Transition in Single Grit Diamond Scribing of Silicon: Application to Wire Sawing of Silicon Wafers, *Journal of Engineering Materials and Technology*, 134, 041011-041011.

Wu, H., Melkote, S.N., Danyluk, S., 2012. Mechanical Strength of Silicon Wafers Cut by Loose Abrasive Slurry and Fixed Abrasive Diamond Wire Sawing, *Advanced Engineering Materials*, 14, 342-348.

Yamada, N., Kim, O.N., Tokimitsu, T., Nakai, Y., Masuda, H., 2011. Optimization of anti-reflection moth-eye structures for use in crystalline silicon solar cells, *Progress in Photovoltaics: Research and Applications*, 19, 134-140.

Yoon, S., Kim, J., Choi, K., 2012. Gettering of metal impurities by using phosphorus diffusion in UMG silicon wafers, *Journal of the Korean Physical Society*, 60, 2079-2082.

Zaidi, S.H., Ruby, D.S., Gee, J.M., 2001. Characterization of random reactive ion etched-textured silicon solar cells, *IEEE Transactions on Electron Devices*, 48, 1200-1206.

Zuschlag, A., Ohl, S., Bernhard, J., Morhenn, H., Ebser, J., Junge, J., Seren, S., Hahn, G., 2010. In: *Proceedings of the Photovoltaic Specialists Conference (PVSC)*, 2010 35th IEEE, pp. 000347-000351.