Temperature dependence of the electrical characteristics up to 370 K of amorphous In-Ga-ZnO thin film transistors

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Abstract:

The temperature dependence in the typical temperature operating range from 300 K up to 370 K of the electrical characteristics of IGZO TFTs fabricated at temperatures not exceeding 200 °C is presented and modeled.

It is seen that up to $T=330$ K, the transfer curves show a parallel shift toward more negative voltages. In both subthreshold and above threshold regimes, the drain current shows Arrhenius-type dependence. In the latter case, for low temperatures, the activation energy is around 0.35 eV for $V_{GS}=10$ V, reducing as V_{GS} is increased. The observed behavior is consistent with having the VRH transport mechanism as the predominant one in conduction.

Keyword: IGZO TFTs, temperature dependence

1. Introduction

Amorphous oxide semiconductor thin film transistors (AOSTFTs) have been dedicated much research work due to their advantages with respect to other types of thin film transistors, TFTs, such as high optical transparency, relatively high electron mobility, as well as low temperature and relatively low cost processing techniques [1-4]. Although the first ZnO TFTs were reported as early as in the 1960s, [5], relatively high mobility and low temperature processing were achieved much later [6].

To increase carrier mobility and device stability, amorphous multi-component oxides have been studied, where several binary oxide components such as Ga_2O_3 , In_2O_3 and HfO_2 are added to the ZnO as base semiconductor. The most successful multi-component oxides are Indium-Gallium-Zinc oxide, (IGZO) and Hafnium-Indium-Zinc oxide, (HIZO). The use of these multi-component oxides has provided a significant reduction in both the bias and light-stress instability [7-9].

In order to understand and describe the properties of the materials, several works can be found, in which the electrical characteristics are analyzed at temperatures below 273 K to determine the conduction mechanisms in AOSTFTs [10-15]. However, results are not conclusive yet, because although several possible mechanisms have been identified, the predominant mechanism will always depend on the specific conditions of the device fabrication processes.

Due to self-heating or to circuit operation conditions, AOSTFTs used in flat panel displays have to work in the temperature range between 243 K and 360 K, according to the temperature specifications of commercial displays. At this

temperature range, however, the AOSTFTs can degrade [16,17]. For this reason, the variation with temperature of their electrical characteristics in the temperature range up to 370 K is also an important piece of information to consider for different applications and should be included in models used for circuit design. In this work we first analyze the temperature dependence up to 370 K of the electrical characteristics of IGZO TFTs fabricated with temperatures processes not exceeding 200 °C, to determine the transport mechanisms present in the devices and to obtain the temperature coefficients of V_T and V_{FB} to be used for modeling their electrical characteristics with temperature. The observed temperature dependence can be well represented, after incorporating the temperature dependence of the model parameters to an AOSTFT model previously developed by our group.

2. Experimental part

The IGZO TFTs were fabricated using a bottom-gate top contacts configuration, as shown in Fig. 1a. For this process, gate metal is patterned on 100 nm of Au deposited on top of 10 nm of Cr (adhesion layer). Both metals were deposited in situ by electron beam. Next, 90 nm of HfO_2 gate dielectric are deposited at 100 °C by atomic layer deposition, followed by 70 nm of IGZO layer, obtained by pulsed laser deposition (PLD) at 20 mTorr oxygen pressure. Immediately after IGZO deposition, devices were annealed in O_2 at 200 °C for 1 hour. The sample is subsequently covered by 500-nm of poly-p-xylylene-C (Parylene-C) protective/hard-mask film deposited by chemical vapor deposition (CVD) at room temperature at 1 mTorr. Gate dielectric vias were opened using photolithographic process and wet etching for the HfO_2 . Source-Drain (S-D) vias were opened through the hard-mask, using O_2 RIE. Then, 100 nm of Al were

deposited by electron beam and patterned to form the *S-D* contacts. Finally, devices were annealed at 100 °C in N₂ for 1 hour. Figure 1b shows an optical micrograph of a typical device. TFTs with different channel widths ($W=40, 80$ and $160\text{ }\mu\text{m}$) and channel length ($L=20, 40$ and $80\text{ }\mu\text{m}$) are included on each die.

Electrical measurements were done in dark, at different temperatures and in vacuum conditions. We used a K20 programmable Temperature Controller and measurement chamber from MMR Technologies Inc. and a Keithley 4200 semiconductor characterization system.

The linear transfer curves and the output characteristics of devices were measured in the temperature range between 300 K and 370 K, which corresponds to a typical operating temperature range. Subsequent measurement cycles were done in order to guarantee that the variation of the drain current was due to the temperature variation and not to instability effects. Since the characteristics for all devices showed a similar behavior, results will be shown for devices with $W=80\text{ }\mu\text{m}$ and $L=40\text{ }\mu\text{m}$.

3. Analysis and discussion of results

Figures 2a and 2b show the experimental data of the linear transfer curve in semilog and linear plot and Fig. 2c show the output characteristics, at room temperature, respectively.

The measurements performed at room temperature were used to determine the set of basic device parameters shown in Table 1. The extraction procedure is described in [18]. Modeled characteristics are also included in Fig. 2 to demonstrate the good agreement between measured and modeled characteristics.

Fig. 3 shows the semi-logarithmic and linear plots of the linear transfer characteristics measured in the range from 300 to 370 K.

To analyze the temperature dependence of the electrical characteristics, the drain current in the above threshold regime I_{DSa} is represented as [18]:

$$I_{DSa}(T) = \left[\frac{K \cdot \mu_{FET}(T) \cdot (V_{GS} - V_T(T)) \cdot V_{DS}}{[1 + K \cdot R(T) \cdot \mu_{FET}(T) \cdot (V_{GS} - V_T(T))]} \right] \cdot \frac{(1 + \lambda \cdot V_{DS})}{\left[1 + \left[\frac{V_{DS}}{\alpha(T) \cdot (V_{GS} - V_T(T))} \right]^m \right]^{1/m}} \quad (1)$$

where

$$\mu_{FET}(T) = \mu_{FET0}(T) \cdot [(V_{GS} - V_T(T))]^{\gamma(T)} \quad (2)$$

$V_T(T)$ is the threshold voltage, $\mu_{FET0}(T)$ is the low field mobility, $\gamma(T)$ is a parameter that describes the dependence of mobility with V_{GS} and T , $\alpha(T)$ is the saturation parameter, m is a parameter related to the knee of the output characteristic before saturation, λ is related to the output conductance increase with V_{DS} , $R(T)$ represents the series resistance, $K = \frac{W}{L} C_i$ and C_i is the gate capacitance per unit area.

In the below threshold regime, two different regions can be distinguished for the drain current. One is the deep subthreshold regime, in which I_{DS} is usually represented as exponentially dependent on the gate voltage:

$$I_{S1}(T) = I_{bo}(T) \cdot e^{\frac{2.3 \cdot [V_{GS} - V_{FB}(T)]}{S(T)}} \quad (3)$$

where $I_{bo}(T)$ is the drain current at the beginning of this region, $V_{FB}(T)$ is the flat band voltage and $S(T)$ is the subthreshold slope.

Between the deep subthreshold regime and the above threshold one, there is another region of subthreshold regime which is represented as:

$$I_{S2}(T) = \left[\frac{(K \cdot [V_{GS} - V_{FB}(T)]^{\gamma_b(T)+1}) \cdot V_{DS}}{V_{bb}^{\gamma_b(T)}} \right] \quad (4)$$

where $\gamma_b(T) = \left(2 \frac{T_o}{T} - 2 \right)$ represents the dependence of the current with V_{GS} in this region; T_o is the characteristic temperature of the localized states and V_{bb} is a model parameter to be extracted.

From eq. (1) to (4) it is evident that the temperature dependence of the drain current in these devices is not simple. Therefore, the temperature behavior is analyzed separately for subthreshold and above threshold regimes.

According to (3), in deep subthreshold regime, the temperature dependence of I_{DS} can be determined by parameters $I_{bo}(T)$, $V_{FB}(T)$ and $S(T)$.

Fig. 3 shows that, as the temperature is increased up to approximately 330 K, the transfer curves show a parallel shift to more negative voltages, indicating a reduction of the flat band voltage with practically no variation of the subthreshold slope.

In Fig. 4, the variation of the I_{DS} for $V_{DS}=0.5$ V and $V_{GS}<3$ V, corresponding to the subthreshold regime, is plotted as function of $1000/T$. The behavior shows an Arrhenius-type dependence with activation energy of around 3.5 eV, which is in the order of the IGZO bandgap. In the same figure, modeled curves using eq. (3) were included to confirm that the behavior matches the experimental data. For modeling, we used the AOSTFT model previously developed by our group and incorporated as level 38 in the simulator Smartspice from SILVACO Inc.

The dependence with temperature of $V_{FB}(T)$ is represented in the form of $V_{FB} = V_{FB0} + KV_{FB}(T - T_0)$, where KV_{FB} for these devices was -0.06 V/K. The variation of V_T with temperature was considered in a similar way as for V_{FB} , where the temperature coefficient is the same.

The reduction of V_T , and consequently of V_{FB} with increasing temperature, has been reported previously for IGZO TFTs and is attributed to either creation of oxygen vacancies or to electron trapping [15,19].

To understand these results we can refer to the following report. In [20], a detailed study on different types of transport mechanisms in amorphous IGZO layers, showed the possibility of having extended band transport including variable range hopping VRH, additionally to the band transport and to the modified band transport. In this latter case, a distribution of potential barriers is considered present inside the conduction band, which hinders carrier transport since carriers with lower energy will have more difficulty to overcome the barriers, therefore, reducing their contribution to the total conduction process. The presence of potential barriers inside the conduction band is attributed to Ga^{3+} and In^{2+} ions. Whether one or another mechanism becomes predominant, will depend on the shape of the distribution of localized states DOS, as well as on the temperature and on the carrier density. Authors demonstrated in [20], that, the contribution of the VRH becomes greater than band-like mechanisms if the Fermi level E_F lies within exponential tail states with a characteristic temperature T_0 around 800 K and a density in the order of $3.4 \times 10^{19} \text{ cm}^{-3}$. They also showed that this effect is more important as the gate voltage decreases. If VRH mechanism is predominant, a linear dependence of the current with the inverse of temperature in a semilogarithmic graphic should be observed.

As seen on Table 1, the value for T_0 was around 830 K and the density of states was around of $8.5 \times 10^{19} \text{ cm}^{-3}$. Therefore, in our case, VRH mechanism seems to be the predominant mechanism. This result is confirmed by the linear dependence of the logarithm of the drain current vs. $1000/T$ observed in Fig. 4. In Fig. 3, it is also observed that, as the temperature is further increased, the device off-current level increases. At 370 K, it is clearly seen that the gate no longer modulates the drain current. The significant increase with temperature of the off-current and lack of gate control on the drain current occurs when the semiconductor layer is thick enough so that full depletion is not achieved. In this case, as the temperature is increased, the density of carriers in the non-depleted semiconductor layer located near the back interface also increases and the parallel current they originate also increases until it becomes predominant [21].

For example, this effect was not present, when we analyzed the behavior with temperature of ZnO TFTs in [22], since the semiconductor thickness was only 40 nm.

Fig. 5 shows the typical behavior of the output characteristic in terms of temperature corresponding to $V_{GS}=10 \text{ V}$. It can be seen that, up to 340 K, the drain current I_{DS} increases with temperature due to the reduction of the V_{FB} and consequently the V_T , maintaining the typical form with the linear and saturation regions.

When the temperature is further increased, the effect of the back region current predominates and the effect of gate channel modulation is lost. The characteristics vary linearly with V_{DS} and saturation is no longer seen.

Fig. 6 shows two regions where the temperature dependence of the logarithm of the drain current in above threshold regime shows a linear dependence with $1000/T$. The activation energy in the region of lower temperatures is in the order of 0.35 eV for $V_{GS}=10$ V and 0.25 eV for $V_{GS}=15$ V confirming that the energy decreases as V_{GS} increases. This is due to E_F moving toward E_C , resulting in a change of the occupancy of the localized states. In the second region, at higher temperatures, the activation energy is around 0.8 eV when V_{DS} is below saturation regime. As V_{DS} enters the saturation regime, the increase in the drain current at high temperatures is more rapid, due to the back conduction becoming more important at high temperatures.

4. Conclusions

The variation with temperature of the electrical characteristics of IGZO TFTs, fabricated with low temperature processes ($T < 200$ °C) has been analyzed in the typical temperature operating range from 300 K up to 370 K. It is seen that up to $T=330$ K, the transfer curves show a parallel shift toward more negative gate voltages. In both subthreshold and above threshold regimes, the drain current shows an Arrhenius-type dependence, with different activation energy, depending on the physical transport mechanism involved. The temperature coefficients for V_T and V_{FB} to model the temperature behavior were found and a good agreement was obtained between measured and modeled plots of the I_{DS} vs. $1000/T$. The variation with temperature of the linear transfer characteristics was also well modeled. In above threshold regime, for low temperatures, an Arrhenius-type dependence is observed with an activation energy of around 0.35 eV for $V_{GS}=10$ V, which reduces as expected to 0.25 eV when the gate voltage is increased to $V_{GS}=15$ V. The observed behavior is consistent with

having the VRH transport mechanism as the predominant one in conduction. As the temperature was further increased, the presence of a back conducting region not controlled by the gate is observed, since the IGZO layer was too thick and full depletion was not achieved. This situation is avoided when the semiconductor layer width is thin enough to guarantee full depletion.

Acknowledgements

This work was supported by CONACyT 237213 project in Mexico, CONACyT interchange programs and NSF/DNDO project ECCS-11139986. M. A. Pavanello acknowledges the Brazilian funding agency CNPq for the financial support.

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Figure caption

Table I Extracted model parameters at T=300 K.

Fig. 1 a) Cross section and b) photo of the device structure.

Fig. 2 Measured at 300 K and modeled a) and b) transfer characteristics in semilog and linear plot, respectively; c) Output characteristics.

Fig. 3 Transfer characteristics measured and modeled in the temperature range from 300 K to 370 K in a) semilog plot with inset showing V_T vs. T and b) linear plot.

Fig. 4 I_{DS} vs. $1000/T$ in the subthreshold regime, measured and modeled using eq. (3).

Fig. 5 Output characteristics for $V_{GS}=10$ V at different temperatures: a) Showing all curves; b) Zoom to show curves up to T=330 K in more detail.

Fig. 6 I_{DS} vs. $1000/T$ in the above threshold regime for $V_{GS}=10$ V and $V_{GS}=15$ V and V_{DS} from 0.5 V to 15 V. The activation energy reduced from 0.35 eV to 0.25 eV at T<330 K, when increasing V_{GS} from 10 V to 15 V.

(a)

(b)

Fig. 1 a) Cross section and b) photo of the device structure.

a)

b

b)

c)

Fig. 2 Measured at 300 K and modeled a) and b) transfer characteristics in semilog and linear plot, respectively; c) Output characteristics.

b

a)

Fig. 3 Transfer characteristics measured and modeled in the temperature range from 300 K to 370 K in a) semilog plot with inset showing V_T vs. T and b) linear plot.

Fig. 4 I_{DS} vs. $1000/T$ in the subthreshold regime, measured and modeled using eq. (3).

a)

b)

Fig. 5 Output characteristics for $V_{GS}=10\ \text{V}$ at different temperatures: a) Showing all curves; b) Zoom to show curves up to $T=330\ \text{K}$ in more detail.

Fig. 6 I_{DS} vs. $1000/T$ in the above threshold regime for $V_{GS} = 10$ V and $V_{GS} = 15$ V and V_{DS} from 0.5 V to 15 V. The activation energy reduced from 0.35 eV to 0.25 eV at $T < 330$ K, when increasing V_{GS} from 10 V to 15 V.

Table I Extracted model parameters at T=300 K.

<i>T</i> [K]	<i>V_T</i> [V]	<i>V_{FB}</i> [V]	<i>μ_{FET0}</i> [cm ² /Vs]	<i>μ_{FET}</i> [cm ² /Vs]	<i>T₀</i> [K]	<i>g_{deep}</i> [cm ⁻³]	<i>γ</i>	<i>γ_b</i>	<i>α_s</i>	<i>m</i>	<i>λ</i>	<i>R</i> [Ω]
300	3.6	2	1.7	7.1	830	8.5x10 ¹⁹	0.6	3.6	0.46	2.27	0	436