Comprehensive Reliability and Aging Analysis on SRAMs within Microprocessor Systems

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Abstract

A framework is proposed to analyze the impact of both Front End of the Line (FEOL) and Back End of the Line (BEOL) wearout mechanisms on memories embedded within state-of-art microprocessors. Our methodology finds the detailed electrical stress and temperature of each SRAM cell within a memory by running a variety of standard benchmarks. Combining the stress/thermal profiles and the wearout models, the performance degradation of SRAM cells for each wearout mechanism is studied. The lifetimes of the SRAM cells are then obtained when the performance metric degrades to a predefined threshold. The proposed work introduces a method to deal with the large volume of SRAM cells whose stress is non-uniform by partitioning the SRAM cells into different stress states, and generates the lifetime distribution of the memory system due to each wearout mechanism by combining the lifetimes of the cells, whose distributions vary with the stress received. Seven wearout mechanisms have been studied, namely, negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), hot carrier injection (HCI), gate oxide breakdown (GOBD), backend dielectric breakdown (BTDDDB), electromigration (EM), and stress-induced voiding (SIV).

1. Introduction

Although technology scaling has resulted in considerable benefits, higher self-heating and electric fields have also contributed to faster aging. The Front End of the Line (FEOL) and Back End of the Line (BEOL) wearout mechanisms degrade SRAM cell stability, margin, and performance, and lead to eventual functional failure. In this paper, a methodology is presented to analyze lifetimes of memories within microprocessors for different wearout mechanisms while running a variety of benchmarks.

The memory lifetime is a function of both FEOL and BEOL wearout.

FEOL lifetime is a function of two kinds of stress: electrical and thermal. As the technology scales, devices undergo increased electrical stress and greater thermal stress. The decrease in device reliability and the increase in SRAM complexity make it very challenging to characterize the SRAM lifetime.

Besides wearout due to FEOL, each technology generation reduces the interconnect dimensions, resulting in higher electric fields within the BEOL dielectric and higher current densities within the metal lines. The increasing wearout in the BEOL geometries and the faster operating frequencies of SRAMs result in decreased interconnect reliability, due to increases in both electrical current and operating temperature.

During SRAM design, it is important to build in design margins to achieve an adequate lifetime. As this has become more challenging, several approaches are proposed to improve SRAM reliability, including circuitry that periodically flips the data in an SRAM cell to reduce failure rates, the use of redundancy, error correcting codes (ECC), and both. Evaluation of these methods requires a model of cell stress. Assumptions are usually made about the stress distribution among cells.

This is because characterizing each SRAM cell based on actual operating conditions is not straightforward. In [1], the authors analyzed the impact of NBTI/PBTI on SRAMs within a microprocessor. However, no explicit SRAM lifetimes were derived and only BTI is discussed.

The purpose of this paper is to present a methodology to assess memory lifetimes due to each wearout mechanism by developing the link between the device level wearout models and the system level. This paper has focused on seven critical wearout mechanisms, namely negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), hot carrier injection (HCI), gate oxide breakdown (GOBD), electromigration (EM), stress induced voiding (SIV) and BEOL time-dependent dielectric breakdown (BTDDDB), and has demonstrated the feasibility of our methodology by presenting results from a lifetime simulator based on the proposed methodology.

Since the wearout mechanisms being studied are activity and temperature dependent, the proposed framework determines the detailed thermal profile of the memory under study, as well as the electrical stress of each net/device in the memory. Combining these profiles and wearout models, the performance degradations of the SRAM cell are studied. In this paper, four performance metrics are considered: read and retention static noise margins (SNMs), write margin, read current (I_{READ}), and the minimum retention voltage ($V_{\text{dd-min}}$). When any of these four performance metrics degrade to a predefined threshold, the SRAM cell is said to have failed and thus the lifetime of this cell is obtained. In order to deal with the large volume of SRAM cells in a memory all of which receive different stress, the cells are partitioned into 21 different stress states, where the cells in each stress state receive the same stress. By this method, the lifetimes of all the cells in the memory due to each

wearout mechanism are determined. Moreover, the lifetime estimates take into account realistic use scenarios [2] which include active, standby, and sleep modes.

The paper is organized as follows. Section 2 presents the wearout models used in this study. Section 3 gives the framework to determine the thermal and electrical stress profiles under use scenarios. Section 4 firstly discusses our methodology to find the performance degradation and lifetime due to NBTI/PBTI and HCI, and then studies the lifetimes of memory due to GOBD, BTDDDB, EM and SIV. Section 6 concludes the paper.

2. Wearout models

2.1. NBTI/PBTI

NBTI and PBTI are generally associated with shifts in the threshold voltage. Recent work has shown that the threshold voltage shift as a function of time under DC stress (t_{DC}) is best modeled with trapping/de-trapping theory [3–6]:

$$\Delta V_{tp/tn}(DC) = \phi_0(A_{BTI} + B_{BTI}\ln(t_{DC}))e^{-E_a/kT}, \quad (1)$$

where, A_{BTI} , B_{BTI} , and ϕ_0 are constants. ϕ_0 is proportional to the number of available traps. The temperature dependence is modeled with the Arrhenius relationship, where E_a is the activation energy, k is a constant, and T is temperature. The duty cycle takes into account the fraction of time under stress and recovery. It modulates ϕ_0 through the Fermi level, which varies as a function of time under stress, t_{str} , and time in recovery, t_{rec} . Hence, overall,

$$\Delta V_{tp/tn} = \phi_0 \left(\frac{t_{str}}{t_{str} + t_{rec}} \right) e^{-E_a/kT} (A_{BTI} + B_{BTI}\ln(t_{str} + t_{rec})). \quad (2)$$

2.2. HCI

The threshold voltage degradation due to HCI during stress is modeled as [7]:

$$\Delta V_{tp/tn} = A_{HCI}(r_{trans}t_{stress}t_{trans})^n \quad (3)$$

where r_{trans} is the frequency-dependent transition rate (transitions per unit time), t_{stress} is the total time under stress/operation, t_{trans} is the transition time (rise or fall time), and A_{HCI} and n are technology-dependent constants that relate to the inversion charge, trap generation energy, and the hot electron mean free path.

2.3. GOBD

Gate oxide breakdown is modelled as a leakage path through the gate oxide [8]. Dielectric degradation and breakdown is modelled with the thermo-chemical model which assumes a direct dependence of oxide degradation on electric field.

For ultra-thin (<5 nm) oxides, the time-to-failure due to gate-oxide degradation can be derived by connecting the oxide degradation model to the Weibull failure distribution function [9] which results in:

$$\eta = A_{ox} \left(\frac{1}{WL} \right)^{\frac{1}{\beta}} e^{-\frac{1}{\beta} V^{a+bT}} \exp \left(\frac{c}{T} + \frac{d}{T^2} \right) s^{-1} \quad (4)$$

where W and L are the device width and length, respectively, η is the time-to-failure for 63.2% of the samples, β is the Weibull shape parameter, $s \in [0,1]$ is the probability of stress, T is temperature, V is gate voltage, and a, b, c, d and A_{ox} are fitting parameters.

2.4. BTDDDB

In order to calculate the vulnerability of a layout to BTDDDB, the BTDDDB simulator operates by breaking the dielectric in each layer and each block into dielectric segments. Each dielectric segment is characterized by a vulnerable length, L_i , and a linespace, S_i . The vulnerable length, L_i , is the length of a block of dielectric between two copper lines separated by linespace S_i . The microprocessor system under study includes 310k nets which form around 31 million dielectric segments. A detailed description of the algorithm is given in [10].

The Weibull characteristic lifetime of a dielectric segment of the microprocessor, with vulnerable length, L_i , associated with linespace, S_i , is

$$\eta = A_{BTDDDB} L_i^{-1/\beta_i} \exp(-\gamma E^m - E_a/kT) \quad (5)$$

where A_{BTDDDB} is a constant that depends on the material properties of the dielectric. E_a is the activation energy (~ 0.5 eV), γ is the field acceleration factor, and m is one for the E model [11] and $1/2$ for the $\sqrt{E}$ model [12]. The electric field is a function of voltage, V , and the linespace, S , between the two lines surrounding a dielectric segment, i.e., $E = V/S$. The electric field (E), temperature (T), and geometry (L_i) determine the characteristic lifetime, η . The temperature dependence is modeled with the Arrhenius relationship [13], where k is the Boltzmann constant. The experimental data used in our study comes from [10].

2.5. EM

EM refers to dislocation of metal atoms caused by momentum imparted by electrical current in interconnects and vias. The vulnerable location is the interconnect/via interface, where a void can form. Specifically, vias are damaged by downstream electron flow from the via to the metal below it. This is because the via and the line below it are formed by separate deposition steps, which creates a vulnerable interface. Hence, although EM can be observed in interconnect lines, it is much more likely to be seen at via interfaces [14–18]. Therefore, this paper focuses on EM in vias, rather than in the significantly less vulnerable interconnect lines. The Weibull characteristic lifetime η of a via due to EM can be modeled as [19]

$$\eta = A_{EM} T / j \quad (6)$$

where T is the temperature, j is the current density, and A_{EM} is a technology-dependent constant that considers the velocity of the void, the resistivity of the metal, surface diffusivity, surface thickness, the thickness of the line, and the via size. The data on EM used in this paper comes from [19].

In order to calculate the vulnerability of a layout to EM, the EM simulator operates by determining the failure time of each interconnect within the microprocessor layout. To better model the reliability of the microprocessor under EM and derive an accurate current density for each interconnect, we collect the activity profiles of each interconnect while running benchmarks and take into account the temperature, RC parasitics and cross-sectional areas of each interconnect.

2.6. SIV

SIV damage is caused by the motion of atoms in interconnects due to mechanical stress caused by the thermal mismatch between metal and dielectric materials. Based on the SIV dependence on both temperature and linewidth of the interconnect above a via, the Weibull characteristic lifetime, η , of a via under SIV is given by [20]:

$$\eta = A_{SIV} W^{-M} (T_0 - T)^{-N} \exp(E_a/kT) \quad (7)$$

where W is the linewidth, M is the geometry stress component, T_0 is the stress-free temperature, N is the thermal stress component, E_a is the activation energy (~ 0.72 eV), and A_{SIV} is a constant. The data used in our study of SIV comes from Yao's experimental data [20].

3. Extraction of activity/thermal profiles

Since the wearout mechanisms under study are activity and temperature dependent, a framework for the acquisition of spatial and temporal thermal/electrical stress of a system was constructed. Running RTL or SPICE simulations of a complete microprocessor to extract the activity profile of each net is not feasible in most cases, since it may take a few months to finish simulating a single benchmark. On the other hand, simulating microprocessors with standard benchmarks on an FPGA (the Xilinx Virtex-5) takes only a few minutes [21–22]. Our framework for extracting the activity/thermal profiles is schematically described in Fig. 1, which provides an efficient way to acquire electrical and thermal profiles of SRAMs within microprocessors for reliability analysis.

For activity tracking, the hardware RTL/netlist of the design under study was synthesized for an FPGA, and counters were placed at the I/O ports of the data cache, which track both the state probabilities and the toggle rates of the ports during application runtime.

The I/O activities and the netlist were then used for activity propagation to each SRAM cell in the data cache for a complete stress/transition probability profile of the SRAM arrays within the microprocessor. Thus, the probability of a transition occurring in any cell and the probability at each state, i.e., the probability at logic "1", are obtained. This provides a complete activity description for each cell within the memory. Fig. 2 shows the distributions of the stress probability and the transition rate of the data cache, when the microprocessor is running a set of standard benchmarks. From the probability at logic "1", we compute the probability of stress due to NBTI, PBTI, GOBD, and BTDDDB, and from the transition rate, we compute the probability of stress due to HCI and EM for each cell within the SRAM.

Besides activity variation, the temperature variation throughout the microprocessor is taken into account when modeling different wearout mechanisms. The netlist was used for layout generation. The RC information from the layout, together with the net activities, was used for the extraction of the power profile and the consequent thermal profile, through the power simulator [23] and the thermal simulator [24], respectively, for every single unit of the microprocessor system. Fig. 3 shows the average temperature distribution when the microprocessor system is running

a standard benchmark.

Then, using the thermal profile and the calculated probability of current flow and voltage stress, the device-level models are used to characterize each wearout mechanism in every SRAM cell of the data cache under study. After the degradation and lifetime of each SRAM cell is estimated, the lifetime distribution of the whole memory is estimated based on the lifetime distributions of each of the cells.

4. Memory lifetime analysis

For analyzing the impact of different wearout mechanisms on SRAM arrays within a microprocessor system, the well-known open-source LEON3 IP core processor [25] with superscalar abilities was used in this work. The microprocessor logic units consist of a 32-bit general purpose integer unit (IU), a 32-bit multiplier (MUL), a 32-bit divider (DIV), and a memory management unit (MMU). Storage blocks include a window-based register file unit (RF), separate data (D-Cache) and instruction (I-Cache) caches, and cache tag storage units (Dtags and Itags). In this paper, we've focused on data cache reliability due to its high activity and temperature [26]. The data cache is a 1024 word $\times$ 32 bit memory, which consists of 32,768 6T SRAM cells.

Four use scenarios [2] are considered in this paper, namely, corporate, general usage, office work, and gaming. The use scenarios have different percentages in active, standby and sleep modes, as shown in Fig. 4.

4.1. Memory lifetime analysis for BTI and HCI

The memory lifetimes due to BTI and HCI are analyzed based on performance degradation. The time-to-failure of each SRAM cell is defined as the time when its performance fails to meet the specifications at normal operating conditions.

Four performance metrics are studied in this paper: the read static noise margin (SNM), the write margin, the read current (I_{READ}), and the minimum retention voltage (V_{dd-min}). The static noise margins are defined as the minimum DC noise voltage necessary to change the state of an SRAM cell. The read SNM is measured with the access transistors turned on, while the access transistors are off for the retention SNM. The write margin is the minimum voltage needed to flip the state of the cell, with the access transistors turned on. V_{dd-min} is the minimum voltage in which the SRAM retains its state. Finally, read current, which is inversely proportional to access time, is the current flow through pull-down devices when performing a read operation. The stability margins were extracted by fitting squared between the static noise margin (SNM) curves and observing the diagonal length of the smaller of the two squares [27].

A set of standard benchmarks were run on the microprocessor system under study. The electrical stress and thermal profiles for the memory were collected by the framework described in Section 3. The realistic use scenarios [2] further modify the stress profile of each cell. The electrical and thermal profiles, process parameter variations, together with the lifetime models from Section 2, were then used to analyze the

performance of each SRAM cell within the memory.

Figs. 5 and 6 show the degradation of read SNM, write margin, read current, and Vdd-min of one SRAM cell due to NBTI, PBTI, and HCI for different use scenarios. The performances are normalized with respect to their specifications and nominal fault free performances, i.e.,

$$Y = (X - X_{spec}) / (X_{fault-free} - X_{spec}) \quad (8)$$

where X is the performance parameter under study, $X_{fault-free}$ is the nominal performance, and X_{spec} is the design specification for fault-free operation.

As our results indicate, for NBTI/PBTI, the minimum retention voltage is most strongly impacted, while the read stability is also severely affected. Both the write margin and read current are relatively unaffected by BTI. Regarding HCI, it improves the read SNM, write margin, and Vdd-min, and degrades I_{READ} .

The framework of estimating the SRAM lifetime due to BTI and HCI is shown in Fig. 7. The thermal profile and activity/stress profile are fed into the BTI/HCI model in Section 2 to obtain the V_{th} degradation. Then SPICE simulations are run to generate the degradation of the four performance metrics. Given the performance constraints, the lifetime of a SRAM cell is then obtained.

In order to manage the large volume of SRAM cells and to limit the number of SPICE simulations, we partition both the static stress probability and switching activity into 21 states for BTI and HCI, respectively. It's assumed that the cells in the same stress state have the same stress. The distributions of stress states for BTI and HCI are illustrated in Figs. 8 and 9, respectively. For each stress state, the flow in Fig. 7 is repeated to get cell lifetimes for both BTI and HCI for each use scenario. The cell lifetimes are then combined with the frequency distribution of stress states to estimate the lifetime of the full memory.

The complexity of this proposed method is $O(N)$, where N is the number of states that the cells are partitioned into.

Figs. 10 and 11 show the distributions of the lifetimes of the 32,768 SRAM cells within the microprocessor due to BTI and HCI, respectively, for different microprocessor use scenarios. Our results indicate gaming has shortest lifetime for both BTI and HCI.

4.2. Memory lifetime analysis for GOBD, BTDDDB, EM and SIV

For GOBD, BTDDDB, EM, SIV, the time-to-failure models from Section 2, together with the thermal and stress profiles collected from the framework proposed in Section 3, are used to characterize the lifetime of each SRAM cell within the memory system under study while taking into account the realistic use scenarios.

The flow to characterize the lifetime of a SRAM cell due to GOBD, BTDDDB, EM and SIV is shown in Fig. 12. Note that the flow is straightforward, using the wearout model in Section 2 to calculate the characteristic lifetime of each cell. The flow of Fig. 12 is repeated for each

SRAM cell and for each use scenario. The complexity is $O(N)$, where N is the number of SRAM cells.

The lifetimes of 32,768 SRAM cells within the microprocessor are obtained. Figs. 13-16 show the lifetime distributions of the SRAM cells within the memory system for different use scenarios. As can be seen from our results, while the lifetimes have smaller deviations over the SRAM cells for GOBD and SIV, the lifetimes are more diverged for the BTDDDB and EM. The results also show gaming has the shortest lifetime for all of these wearout mechanisms. Of course, the lifetimes depend on the technology constants used in the analysis.

5. Conclusion

A simulation methodology to analyze memory reliability for both FEOL and BEOL wearout mechanisms has been proposed. Combining the wearout models, the thermal profiles, and the electrical stress profiles, the performances of memory cells under non-uniform stress can be evaluated more accurately. This work provides insights on memory reliability under real use conditions and could be extend to STT-MRAM in future work [28–29].

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References

- [1] C.-C. Chen, F. Ahmed, L. Milor, "Impact of NBTI/PBTI on SRAMs within microprocessor systems: Modeling, simulation, and analysis," *Microelectronics Reliability*, vol. 53, pp. 1183-1188, 2013.
- [2] R. Kwasnick, A.E. Papathanasiou, M. Reilly, A. Rashid, B. Zaknoon, and J. Falk, "Determination of CPU use conditions," *Proc. IRPS*, 2011, pp. 2C.3.1-2C.3.6.
- [3] G.I. Wirth, R. da Silva, and B. Kaczer, "Statistical model for MOSFET bias temperature instability component due to charge trapping," *IEEE Trans. Electron Devices*, 2011, vol. 58, no. 8, pp. 2743-2751.
- [4] C.-C. Chen, S. Cha, T. Liu, and L. Milor, "System-level modeling of microprocessor reliability degradation due to BTI and HCI," *IEEE IRPS*, pp. CA.8.1-CA.8.9, 2014.
- [5] S. Cha, C.-C. Chen, T. Liu and L. Milor, "Extraction of threshold voltage degradation modeling due to Negative Bias Temperature Instability in circuits with I/O measurements," *IEEE VLSI Test Symposium*, pp. 1-6, 2014.
- [6] G. Gielen, *et al.*, "Emerging yield and reliability challenges in nanometer CMOS technologies," *Proc. DATE*, 2008, pp. 1322-1327.
- [7] W. Wang, *et al.*, "Compact Modeling and Simulation of Circuit Reliability for 65-nm CMOS Technology," *IEEE Trans. Device and Materials Reliability*, 2007, vol. 7, no. 4, pp. 509-517.
- [8] X. Li, *et al.*, "Compact Modeling of MOSFET wearout mechanisms for circuit-reliability simulation," *IEEE Trans. Device and Materials Reliability*, 2008, vol. 8, no. 1, pp. 98-121.
- [9] C.-C. Chen, S. Cha and L. Milor, "System-level modeling of microprocessor reliability degradation due to TDDDB," *Conference on Design of Circuits and Integrated Systems*, 2014.
- [10] C.-C. Chen, M. Bashir, L. Milor, D.H. Kim, and S.K. Lim, "Backend dielectric chip reliability simulator for complex interconnect geometries," *IEEE IRPS*, pp. BD.4.1-BD.4.8, 2012.
- [11] G. S. Haase, *et al.*, "Modeling of interconnect dielectric lifetime under stress conditions and new extrapolation methodologies for time-dependent dielectric breakdown," in *Proc. IRPS*, pp. 390-398, 2007.

- [12] F. Chen, *et al.*, "A comprehensive study of low- k SiCOH TDDDB phenomena and its reliability lifetime model development," in *Proc. IRPS*, pp. 46–53, 2006.
- [13] K.-Y. Yiang, *et al.*, "TDDDB kinetics and their relationship with the E- and $\sqrt{E}$ - models," in *Proc. IITC*, 2008, pp. 168–170.
- [14] C.-C. Chen and L. Milor, "Microprocessor Aging Analysis and Reliability Modeling Due to Back-End Wearout Mechanisms," *IEEE Trans. Very Large Scale Integration (VLSI) Systems*, 2014.
- [15] C.-C. Chen and L. Milor, "System-level modeling and microprocessor reliability analysis for backend wearout mechanisms," *Proc. DATE*, pp. 1615–1620, 2013.
- [16] C.-C. Chen, M. Bashir, L. Milor, D.H. Kim, and S.K. Lim, "Simulation of system backend dielectric reliability," *Microelectronics Journal*, 2014.
- [17] C.-C. Chen, F. Ahmed, D. H. Kim, S. K. Lim, L. Milor, "Backend dielectric reliability simulator for microprocessor system," *Microelectronics Reliability*, vol. 52, pp. 1953–1959, 2012.
- [18] M. Bashir, C.-C. Chen, L. Milor, D.H. Kim, and S.K. Lim, "Backend dielectric reliability full chip simulator," *IEEE Trans. VLSI Systems*, vol. 22, no. 8, pp. 1750–1762, August 2014.
- [19] Z.-S. Choi, *et al.*, "Activation energy and prefactor for surface electromigration and void drift in Cu interconnects," *J. Appl. Phys.*, vol. 102, no. 8, pp. 083509-1–083509-4, 2007.
- [20] H. W. Yao, *et al.*, "Stress migration model for Cu interconnect reliability analysis," *J. Appl. Phys.*, vol. 110, no. 7, pp. 073504-1–073504-5, 2011.
- [21] C.-C. Chen, F. Ahmed, and L. Milor, "A Comparative Study of Wearout Mechanisms in State-of-Art Microprocessors," *Proc. IEEE ICCD*, pp. 271–276, 2012.
- [22] C.-C. Chen, and L. Milor. "System-level modeling and reliability analysis of microprocessor systems." *IEEE International Workshop Advances in Sensors & Interfaces*, pp. 178–183, 2013.
- [23] PrimeTime power modeling tool: www.synopsys.com.
- [24] HotSpot: lava.cs.virginia.edu/HotSpot.
- [25] LEON3 processor: www.gaisler.com.
- [26] C.-C. Chen and L. Milor, "System-level modeling and microprocessor reliability analysis for backend wearout mechanisms," *Proc. DATE*, 2013.
- [27] E. Seevinck, F.J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.
- [28] Jing Li, Haixin Liu, Sayeef Salahuddin and Kaushik Roy, "Variation-Tolerant Spin-Torque Transfer (STT) MRAM Array for Yield Enhancement", *IEEE Custom Integrated Circuits Conference (CICC)*, 2008.
- [29] Jing Li, Patrick Ndai, Ashish Goel, Haixin Liu and Kaushik Roy, "An Alternate Design Paradigm for Robust Spin-Torque Transfer Magnetic RAM (STT MRAM) from Circuit/Architecture Perspective", *Asia and South Pacific Design Automation Conference (ASP-DAC)*, 2009.

Figure 1

Fig. 1. The schematic of the electrical/thermal extraction framework.

Figure 2

Fig. 2. The distributions of the stress probability (part (a)) and the transition rate (part (b)) for the data cache while running a set of standard benchmarks.

Figure 3

Fig. 3. The average temperature distribution of the microprocessor.

Figure 4

Fig. 4. The percentages of different use scenario in active, standby and sleep modes [2].

Figure 5

Fig. 5. The degradations of all the performance metrics due to NBTI/PBTL.

Figure 6

Fig. 6. The degradations of all the performance metrics due to HCI.

Figure 7

Fig. 7. The flow of estimating the lifetime of a SRAM cell due to BTI and HCI.

Figure 8

Fig. 8. The distribution of the number of cells in each stress state.

Figure 9

Fig. 9. The distribution of the number of cells in each toggle-rate state.

Figure 10

Fig. 10. The distributions of the lifetimes of the SRAM cells due to PBTI/NBTI.

Figure 11

Fig. 11. The distributions of the lifetimes of the SRAM cells due to HCI.

Figure 12

Fig. 12. The flow of estimating the lifetime of a SRAM cell due to GOBD, BTDDDB, EM and SIV.

Figure 13

Fig. 13. The distributions of the lifetimes of the SRAM cells due to GOBD.

Figure 14

Fig. 14. The distributions of the lifetimes of the SRAM cells due to BTDDDB.

Figure 15

Fig. 15. The distributions of the lifetimes of the SRAM cells due to SIV.

Figure 16

Fig. 16. The distributions of the lifetimes of the SRAM cells due to EM.