22 μm -Pitch 9-bit Column-Parallel Overlapping-Subrange SAR (CPOSSAR) ADC

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Abstract

The Column-Parallel Overlapping-Subrange Successive-Approximation-Register Analog-to-Digital Converter (CPOSSAR ADC) uses a 5-bit split capacitor DAC twice to achieve 9-bit resolution. Its total capacitor area is only 3% of a 9-bit binary weighted DAC and the average switching power is only 12% of a conventional 9-bit DAC. The ADC can perform a 9-bit conversion by first digitizing the 4 most significant bits (MSB) in a coarse conversion stage and then digitizing the 5 least significant bits (LSB) in a fine conversion stage. The accuracy requirement of the DAC is reduced by using overlapping subranges. The proposed ADC achieved an SFDR of 73.6 dB and a SINAD of 55 dB in post-layout simulation, corresponding to an ENOB of 8.8 bits. The design was fabricated in TSMC's 0.35 μm high-voltage process. The use of overlapping subranges reduced the DNL error from +5.14/-1 LSB to +1.27/-0.92 LSB, and improved the INL error from +5.35/-5.34 LSB to +3.17/-3.18 LSB. At a sampling rate of 1.1 MS/s the ADC achieved 41.5 dB SFDR, 34.2 dB SINAD, and consumed 242 μW /channel dynamic power. An individual ADC channel is only 22 μm wide. CPOSSAR ADCs are a factor of 4, 2, and 2.5 more area efficient than Multiple-ramp Single-slope ADCs, SAR ADCs, and Cyclic ADCs.

Key words: Column-parallel analog-to-digital converter; SAR ADC; Overlapping subranges; Calibration; CMOS active pixel sensors;

1. Motivation

Column-parallel ADCs are frequently used in CMOS imagers to achieve fast frame rates. The key parameters for the design of these ADCs include area, pitch, speed, and quantization resolution. The single-slope architecture is often used because of the simple circuitry in each channel. But the conversion rate for this type of ADC is usually less than 1 MSPS, because the full-scale conversion time doubles with each additional bit [1], [2]. In comparison, successive approximation register (SAR) ADCs can perform faster conversions at moderate to high resolution because the conversion time scales linearly with the number of bits. The disadvantage of SAR ADCs, however, is that they rely on a DAC to produce reference voltages. Usually a high-resolution high-linearity SAR ADC requires a large silicon area for capacitors in the DAC,

making it unsuitable for column-parallel applications.

One way to mitigate the large area requirement of SAR ADCs is to use the subranging technique. First a coarse conversion is performed to determine the M most significant bits. Then a fine conversion is performed over the subrange determined by the coarse conversion to calculate the K least significant bits. One way of implementing this second conversion is using a capacitor-array DAC to resolve voltages between two reference voltages that are generated with a resistor ladder [3]. When building an array of column-parallel ADCs, this resistor ladder can be shared by all of the channels. The area can be further reduced by using the same capacitor-array DAC to perform both the coarse and fine conversions, but in order to guarantee a correct coarse conversion for any inputs, the DAC must be accurate to the full resolution of the conversion ($M+K$).

CPOSSAR ADCs perform a 9-bit conversion by using a 5-bit SAR ADC twice, without requiring that the 5-bit ADC be 9-bit accurate by using overlapping subranges. The coarse conversion is performed by a 5-bit capacitor DAC to determine $D[9:5]$. Then $D[9:6]$ is used to select a subrange provided by a 4-bit global resistor ladder. The fine-stage conversion is then performed inside the selected subrange to determine $D[4:0]$. $D[5]$ is used as part of the proposed overlapping subrange scheme.

2. Subranging SAR ADC with overlapping references

2.1 Concept of Subranging SAR ADC

The 9-bit subranging SAR ADC achieves higher resolution than is conventionally possible from its 5-bit ADC by adapting into a smaller reference rail during the fine conversion stage. Fig. 1 depicts the operation of the subranging method. During the coarse conversion stage, V_{capH} is set to the maximum of the conversion range and V_{capL} is set to the minimum. The upper five bits, $D[9:5]$, are resolved through the successive approximation process. During the fine stage, $D[9:6]$ is decoded to select which one of the subranges includes the input voltage. The corresponding high reference voltage, $V_{\text{ref}(i+1)}$, and low reference voltage $V_{\text{ref}(i)}$, are then assigned independently in each channel. A 5-bit successive approximation process is performed again to determine the lower 5 bits, $D[4:0]$. Finally $D[9:6]$ and $D[4:0]$ are concatenated for a complete result.

Fig. 1. The subranging SA conversion process involves two stages. In each stage successively better approximations of the input signal are generated by comparing the input voltage with a DAC generated voltage. In the coarse conversion stage, the two reference

voltages for the DAC are set to the minimum and maximum of the full conversion range. One bit is determined at a time from the MSB to the LSB of the DAC. The result of this coarse conversion is then used to select two new reference voltages for the DAC during the fine conversion stage. Since these reference voltages are closer together, the voltage swing associated with each bit of the DAC is reduced.

2.2 Advantage of Overlapping Subranges

In the standard subranging topology, the coarse conversion must be performed to the full accuracy of the final conversion. Using a 5-bit ADC twice to build a 9-bit subranging SAR ADC, an example of this requirement is differentiating between 00001111_2 and 00010000_2 . Because the two codes are located on either sides of the transition point (boundary) between two connected subranges (0000_2 and 0001_2), a small mismatch of the transition voltage, due to DAC mismatch, will digitize the input voltage into an incorrect subrange. So the coarse conversion needs to determine the upper 4 bits to 9 bits accuracy in order to select the correct subrange for the fine conversion. The larger devices required to assure this higher level of matching reduce the area savings that the subranging topology is designed to achieve. An accurate conversion can be performed with less accurate ADCs by utilizing the redundancy in a 3.5-bit thermometer code ADC to achieve 3 bits in coarse conversion [4] or splitting the capacitors in coarse conversion DAC to digitally correct coarse conversion error [5], but both of these techniques increase circuit area and introduce complicated switching algorithms. CPOSSAR ADCs use a simple level shifter driven by the LSB of the coarse conversion result to reduce the accuracy requirement from 9 bits to 5 bits.

Fig. 2(A) illustrates an example of the incorrect subrange selected in fine stage and how a raised subrange can avoid such error. In this example the 4-bit resistor ladder is assumed to be more than 9-bit ratio-accurate. This can be guaranteed by dedicatedly designing a large common-centroid double-poly resistor in the targeted technology. The area budget is less critical in this scenario because the resistor ladder is shared globally. During the coarse conversion stage, the full reference scale ($V_{capL} \sim V_{capH}$) is used and one LSB voltage, V_{LSB} , is defined as $(V_{capH} - V_{capL})/512$ corresponding to final 9-bit resolution. Nonlinearities of the 5-bit ADC correspond with a few V_{LSB} errors for some or all reference points in this full scale. So the capacitor related reference voltage, $V_{cap_actual2}$, vary from the ideal value, V_{cap_ideal2} , which aligns with the mismatch-free resistor ladder created reference voltage, V_{ref2} . For a simple demonstration, assume the lower reference voltages, $V_{cap_actual1}$, V_{cap_ideal1} , and V_{ref1} , are aligned. An input, V_{in} , corresponding to digital word 192_{10} is waiting for conversion. In the case depicted in Fig. 2(A), V_{in} resides in an ideal subrange corresponding to $D[9:6]=0110_2$, but is digitized as 0101_2 due to the higher $V_{cap_actual2}$ than V_{cap_ideal2} . In addition, $D[5]$ is 1 since V_{in} is located at the upper half of the erroneous subrange, from $V_{cap_actual1}$ to $V_{cap_actual2}$. For the fine stage, instead of selecting subrange $D[9:6]=0110_2$, the lower subrange $D[9:6]=0101_2$ will be selected. If the sub-range voltages provided by the resistor ladder are simply passed to the 5-bit ADC, fine conversion will return 1111_2 for $D[4:0]$ because V_{in} exceeds the top of the selected subrange. The overall conversion result will be 191_{10} , resulting in 1 LSB error. This error is solely induced from the coarse conversion stage and cannot be fixed unless the incorrect subrange used in fine stage is detected and corrected. The error can be more than 1 LSB if $V_{cap_actual2}$ is higher than V_{cap_ideal2} by more than

1 V_{LSB} .

Fig.2 (A) This example shows the subrange used in fine conversion stage will be incorrect if the actual reference voltage, $V_{cap_actual2}$, generated from the capacitor DAC in 5-bit ADC differs from its ideal value, V_{cap_ideal2} . So the input will exceed the ceiling of the selected subrange and error is induced. But when the raised subrange is introduced, the input is guaranteed to be covered by the reference range, so the error is avoided. (B) For all other inputs between 160 and 191, if it is located at the lower half of the erroneous subrange, the unraised subrange will be used, otherwise the raised subrange is used and an offset of 16 LSB is added to the concatenated result. In both cases no error exists because the input is always assured to be covered by the reference range.

The error originates from the fact that input voltages may exceed the fine conversion reference rail due to incorrect selection of the subrange. To avoid such effect, a raised subrange shown in Fig. 2(A) is useful. As D[5] in coarse conversion is 1, the corresponding resistor ladder created subrange is raised by an offset of ΔV , or $16V_{LSB}$, so that the raised subrange straddles right in the middle of two connected subranges produced by the resistor ladder. V_{in} is now at the upper half of the raised subrange, so D[4] is 1 and the lower bits are D[3:0]=0000₂. After the concatenation, an offset of 16 LSB is added to 01010000₂, resulting in 011000000₂, which is the correct digital value of V_{in} .

As is shown in Fig. 2(B), when the input, V_{in} , is at the bottom of the erroneous subrange, corresponding to 160₁₀, the unraised subrange will not cause error because V_{in} is still inside the selected subrange. This is also true if V_{in} is lower than V_{cap_ideal2} by less than 1 LSB voltage, corresponding to 191₁₀. But as it is located at the upper half of the erroneous subrange, D[5] is 1 and the raised subrange is used in fine conversion for algorithm consistency. In that case D[4:0] is 01111₂. After the concatenation an offset of 16 V_{LSB} is added, resulting in 01011111₂. All other inputs between 160₁₀ and 191₁₀ are converted in the same manner without causing errors by selecting a correct subrange in fine conversion stage. The shifting in voltage domain will be recovered in digital domain by adding the 16 LSB offset.

Shifting the subrange up when D[5] equals 1 is sufficient to avoid errors at the high end of the subrange and a shift down to avoid errors at the low end of the subrange would be possible, but a simpler solution is to shift the unshifted subranges as shown in Fig. 3(A). Two sets of subranges are created, overlapping each other. In order to make this shifting method useful for all subranges, the resistor ladder reference range, V_{resH} to V_{resL} , is set to be lower than the coarse conversion reference range, V_{capH} to V_{capL} , so that $V_{ref(i)}$ is not higher than $V_{cap_actual(i)}$ for $i=0\sim15$. The resultant voltage alignment pattern can be generalized in Fig. 3(B). Noticing that ΔV_1 does not necessarily equal to ΔV_2 due to the fact that the

1 mismatch of the capacitor DAC does not have the same error effect for all reference points.

Fig. 3 (A) Each reference voltage created by the resistor ladder is shifted up by half an ideal subrange, $16 V_{LSB}$, to produce raised subranges. Two sets of subranges overlap each other and are alternatively used for different inputs. (B) Each resistor ladder created reference voltage, $V_{ref(i)}$, is assured to be no higher than the corresponding capacitor created reference voltage, $V_{cap_actual(i)}$, to make the overlapping subranges useful across the entire conversion range.

The fundamental principle behind the overlapping subrange is to extend the effective width of an ordinary subrange, so that input voltages close to the boundary will always be covered by either the raised or unraised subrange in the fine conversion stage. A 5-bit ratio-accurate capacitor DAC limits the variation of $V_{cap_actual(i)}$ from $V_{cap_ideal(i)}$ by $\pm 8 V_{LSB}$. In the worst cases, input voltages corresponding to $V_{cap_ideal(i)} \pm 8 V_{LSB}$ are digitized into incorrect sub-ranges in coarse conversion stage, resulting in ± 8 LSB error. Shifting the subranges by $16 V_{LSB}$ upwards will assure the problematic inputs do not exceed the reference rail in fine conversion stage for all cases, so that incorrect coarse conversion can be tolerated. Compared to a conventional 9-bit SAR ADC, this method reduces the 9-bit ratio-accuracy requirement on capacitor DAC down to 5 bits. This accuracy relaxation applies to other resolution topologies. For example, the 7-bit coarse and 6-bit fine CPOSSAR ADCs only require 7-bit ratio accurate capacitor DAC to achieve 13-bit overall resolution. However, conversional 13-bit SAR ADCs and Cyclic ADCs require their capacitor matching inside each channel no less than 13-bit. The protocol for shifting the subranges and post-processing the concatenated conversion result is shown in Fig. 4. After the coarse stage, the unraised subrange is used if $D[5]$ is 0. Data is concatenated without adding any offset. When $D[5]$ is 1, the raised subrange is used and an offset of 16 LSB is added, recovering the shifted voltage. This error calibration process is performed in analog domain with any digital logics.

Fig. 4 The raised subrange is used only if $D[5]$ is 1 in coarse conversion. An offset of 16 LSB will be added to the concatenated result. When $D[5]$ is 0 the unraised subrange is used and no offset is added.

3. Circuit Implementation

3.1 System architecture

We implemented the CPOSSAR ADCs using the conventional technique of a resistor ladder to generate subrange reference voltages [6] and a capacitor-array SAR ADC for the conversion. The resistor ladder is shared globally across all columns, as shown in Fig. 5. This 4-bit resistor ladder provides 16 monotonic subranges. Inside each channel, a conventional SAR architecture consisting of a 5-bit capacitor-array DAC, a differential amplifier, a dynamic comparator, and a successive approximation register performs both the coarse and fine conversions. The coarse conversion result, $D[9:5]$, is stored in a 5-bit register at the end of the coarse stage. The upper 4 bits, $D[9:6]$, are used during the fine stage to control a pair of bias switches that select the subrange, which is then shifted up by the level shifter if required.

Fig. 5. The block diagram of the CPOSSAR ADC shows that the resistor ladder is shared by all of the columns and each column includes bias switches, a level shifter, a capacitor array DAC, an amplifier, a dynamic comparator, a 5-bit successive approximation register, and a 5-bit register.

3.2 5-bit DAC

The DAC used in the 9-bit CPOSSAR ADC is built using a 5-bit capacitor array, which implements the split capacitor technique to further reduce the area, as shown in Fig. 6. Each capacitor is implemented with a Poly-Insulator-Poly capacitor and is composed of an integer number of the design-rule-restricted minimum unity capacitors, C_0 (~13.75 fF). The smallest capacitor, corresponding to $d[2]$ in Fig. 6, was made by 7 unity capacitors, with a total capacitance of ~100 fF and a total area of 21 μm by 13 μm .

The KT/C noise associated with the capacitor is $200 \mu V$ (at $300 K$), or 10% of V_{LSB} , $\sim 2 mV$. The total capacitance of the capacitor array is $113 C_0$, only 3% of the capacitance of a 9-bit binary weighted capacitor array ($3584 C_0$). The average switching energy of the binary weighted 9-bit DAC is [7]

$$E_{bin9} = \sum_{i=1}^9 (2^{N+1-2i})(2^i - 1)(7C_0)V_{fs}^2 \quad (1)$$

where N equals 9 and V_{fs} is the full reference range in coarse-stage conversion, $V_{capH} \sim V_{capL}$. The corresponding expression for the 5-bit DAC is

$$E_{split} = (1 - \alpha) \sum_{i=1}^5 (2^{N+1-2i})(2^i - 1)(14C_0)(1 + \frac{1}{16^2})V_{fs}^2 \quad (2)$$

where N is 5 and α equals 0.37 to account for the energy savings from the split capacitor technique [8]. As shown by comparing (1) and (2), the design reduces the energy consumption by 88% compared to a conventional 9-bit binary weighted DAC.

Fig. 6 The 5-bit capacitor DAC is implemented using the split capacitor topology to save the area. The circuit is integrated with sampling function (assisted by the subsequent amplifier) and reference voltage multiplexing function through the use of two analog multiplexers (Switch A) and an OR gate.

Common-centroid capacitor layout would minimize the mismatch from process variation, but it dramatically increases the complexity of the layout and the wire length in the narrow channel of each column. Instead, the effect of parasitics was minimized by optimizing interconnections using post-layout extraction.

The capacitor-array DAC operates by switching the voltages on the bottom plates of the binary weighted capacitors. Each capacitor can be connected to the input voltage for sampling, to the high reference to set a logic “1”, or to the low reference to set a logic “0.” Switching between these values is performed using $2.4 \mu m/0.35 \mu m$ NMOS transistors with $7 k\Omega$ average on resistance. Transmission gate switches would increase the voltage swing to full power supply rail, but it necessitates rail-to-rail operation of op amps, and analog switches’ control signals in all other blocks should be complementary. Implementing such design complexity in op amp, bias switch circuit, and layout routing in the narrow channel was proven to be uneconomical from performance-area point of view. This makes transmission gate unnecessary in capacitor-array DAC. The largest switching step corresponds to MSB, $D[9]$, in coarse stage. The time constant, τ , associated with this bit was $1.35 ns$ according to post-layout simulation, so that

1 in 9.45 ns, 7 time constants, the capacitor array output settles down to the final value with less than 0.1 %
2 error, or $0.256 V_{LSB}$. An entire conversion takes 36 times this long, or 18 clock cycles, corresponding to
3 over 1 MS/s. A further increase in speed could be achieved by allowing less settling time for lower bits
4 since the step size is smaller, but the added complexity was deemed unnecessary for this application.

5 *3.3 Amplifier and Comparator*

6 A single circuit serves as both the amplifier for sampling the input onto the capacitors of the DAC
7 during sample mode and as a clocked comparator during conversion mode. The configuration of the circuit
8 is switched between these roles to ensure stable operation in feedback during sample mode and maximum
9 gain and speed as an amplifier during conversion mode. The operation in the sample mode is described
10 first and then the comparator function is described.

11 *3.3.1 Amplifier and S/H mechanism*

12 The amplifier operates in feedback mode to sample the input voltage onto the capacitor array of
13 the 5-bit DAC at the beginning of each conversion. The amplifier circuit used in the CPOSSAR ADC is
14 shown at the top of Fig. 7. In this sub-circuit, the first stage uses a PMOS differential pair to sense the
15 voltage difference. The differential current is mirrored to the second stage with a gain of 4 and drives a
16 cross-coupled active load consisting of $M_1 \sim M_4$. A cascoded amplifier amplifies one output from the load
17 and feeds back this voltage into V_- through a 800 nm/ 350 nm NMOS switch ($4.5 \text{ k}\Omega$ on resistance)
18 controlled by the sampling clock, Clk_spl . During the sampling, V_+ is biased at a fixed common mode
19 voltage, V_{cm} , and the output of the capacitor array, V_{out_cap} , is connected to V_- . While Clk_spl is high, the
20 negative feedback tracks the input and the differential pair offset is stored on the capacitor. When Clk_spl
21 toggles to ground, the capacitor array output becomes a high impedance node and the trapped charge is
22 redistributed among capacitors for the subsequent conversion.

Fig. 7 The amplifier and the clocked dynamic comparator are cascaded. The amplifier samples the input onto the capacitor array of the DAC when connected in a feedback loop. It pre-amplifies the input in open-loop and reduces the input offset of the dynamic comparator by a factor of 40. The clocked comparator consists of two clocked stages and a latch stage. Its kickback noise can be isolated from the 5-bit DAC by the amplifier stage.

In the amplifier, the PMOS differential pair is separated from the active load to split a low frequency pole into two high frequency poles to improve the speed. Both pole frequencies are higher than 120 MHz as determined by hand calculation and verified by post-layout simulation.

The active load is made up of two cross-coupled PMOS transistors, M_1 and M_2 , and two diode-connected PMOS transistors, M_3 and M_4 . The cross-coupled transistors exhibit negative differential-mode resistance and the diode-connected transistors offer small positive output resistance. The parallel connection of two types of loads essentially adds a large positive conductance and a slightly smaller negative conductance. As is demonstrated by equation (3), with appropriate transistor scaling, the total differential-mode output resistance can be increased. So the open-loop gain of the pre-amplifier is improved. As shown by equation (4), the common-mode output resistance is small. This creates a low common-mode gain ensuring that the amplifier remains stable without adding common-mode feedback.

The amplifier was characterized using post-layout simulation in both sample and conversion modes. In sample mode, the closed-loop unity-gain bandwidth is 114 MHz and the phase margin is 56° . The low-frequency open-loop gain is 67 dB and the phase margin is 22° . The finite gain induced maximum sampling error is 416 μ V, or $0.2 V_{LSB}$. In conversion mode the low frequency differential open-loop gain is 32 dB (40V/V). The -3 dB bandwidth is 36 MHz (loaded with subsequent circuits) and the phase margin is 30° . The pre-amplification is used in the conversion mode to improve the accuracy of the

subsequent clocked dynamic comparator. It also reduces the kick back noise seen by the capacitor DAC from the dynamic comparator.

$$r_{load,diff} = \frac{2}{g_{m3,4} - g_{m1,2}} \quad (3)$$

$$r_{load,CM} = \frac{1}{2(g_{m1,2} + g_{m3,4})} \quad (4)$$

3.3.2 Clocked dynamic comparator

The comparator includes two clocked stages and an SR latch. It was inspired by the dynamic comparator used in a charge-redistribution ADC [9]. When the comparison clock, Clk_comp, is low, both clocked stages are turned off with both outputs of the clocked stage 1 pre-charged to the power supply, V_{dd} , and both outputs of the clocked stage 2 pulled down to ground. When Clk_comp rises, the outputs of the clocked stage 1 fall at different rates based on the pre-amplified input voltage. The clocked stage 2 then utilizes the cross-coupled inverters to compare these two voltages. In order to improve the speed of the cross-coupled latch, two inverters ($M_5 \sim M_8$) were added to form feedback loops that drive the drain of input transistors, M_9 and M_{10} , pulling them out of saturation. The feedback inverters' layouts are common-centroid to ensure the equivalent speed-up for both sides. The final stage is an SR latch that holds the comparison result from the previous comparison when Clk_spl is low.

Offset of the dynamic comparator can be effectively reduced by tuning the bulk voltage of the PMOS input transistors[10], [11]. In the proposed topology, the offset of the differential amplifier is sampled onto the capacitor DAC during sample mode. In conversion mode, its pre-amplification gain reduces the subsequent dynamic comparator offset by a factor of 40.

3.4 Level shifter

The level-shifter circuit initially samples the reference voltage on a capacitor. Shifting is then performed by raising the bottom plate of the capacitor by a fixed offset during the hold phase. The schematic of the level shifter is presented in Fig. 8. Input and output buffers stand on either side of a sampling/hold circuit built with an NMOS switch and a 0.5 pF capacitor. During the sampling stage, Φ_1 is high and Φ_2 is low. The bottom plate of the sampling capacitor is biased at a voltage named V_{bias} . The top plate of the capacitor tracks the selected reference voltage because M_1 is conducting. When the two clock signals toggle states, the top plate of the sampling capacitor becomes a high impedance node trapping the charges. Depending on the state of D[5] determined during coarse conversion, the bottom plate of the sampling capacitor is either driven to a voltage named $V_{bias} + \Delta V$, or remains unchanged. In the first case the top plate voltage will be raised by ΔV , creating a shifted reference voltage at the output. Charge injection effect was minimized by including a dummy transistor, M_2 , half as wide as M_1 . Clock Φ_2 is delayed from clock Φ_1 to ensure that the M_1 is switched off completely before the bottom plate voltage of the sampling capacitor is changed by the analog multiplexer named Switch B.

Fig.8 The level shifter is built with a capacitor sampling and hold circuit and two buffers. The sampling and hold circuit is able to shift its output by implementing an analog multiplexer (Switch B) that changes the bottom plate potential of the sampling capacitor.

3.5 Subrange decoding and bias switching

The subrange selection is performed based on $D[9:6]$ determined in the coarse conversion. In Fig. 9, 16 reference voltages are generated by the global 4-bit resistor ladder. These voltages and the high reference voltage used in the coarse stage, V_{capH} , are buffered and routed to a 17-channel reference bus shared by all columns. Each pair of sub-range voltages is switched by a pair of NMOS transistors controlled by a 4-bit decoder. Again, transmission-gate switches were not used because routing complementary signals in a 22 μm wide layout takes considerable area, but it contributes insignificantly to the performance due to the non-rail-to-rail op amps implemented in the prototype.

Fig. 9 The sub-range voltages are created by cascading 16 identical resistors and are buffered to a 17-channel reference bus shared by all columns. In the front end of each column ADC, bias switches select one of the subranges by closing a pair of NMOS transistors that are controlled by a sub-range decoder.

3.6 Zero-offset global reference buffer

While having a more than 9-bit ratio-accurate resistor ladder to generate subrange voltages is the basic accuracy requirement for fine conversion, delivering those references to each column ADC requires proper buffering without offset error. The standard offset sampling technique was used to minimize the error [12].

Fig. 10 The offset sampling technique is used to reduce the offset error of the reference buffer. The offset voltage is first stored on the sampling capacitor and then canceled out by connecting the capacitor in the feedback loop.

As is shown in Fig. 10, when the switch controlled by Φ_1 closes, both the output and the inverting input of the op amp are driven to a voltage equal to V_{in} plus the offset voltage. When the second switch controlled by Φ_2 closes, the bottom plate of C_s , a 0.48 pF capacitor, is connected to V_{in} so that the offset voltage is tracked on C_s . Finally, the switches controlled by Φ_1 and Φ_2 are opened trapping charge on C_s , and the switch controlled by Φ_3 is closed to form the feedback loop. In this mode the offset voltage is canceled out. Since the buffered reference voltage is shared by all columns, the amplifier was implemented with a folded-cascoded op amp and a class AB output stage for sufficient loading capacity.

3.7 Layout and floorplan

One of the primary constraints for this ADC design is the narrow layout to enable the integration of a large number of ADCs with a CMOS active pixel sensor array. The pitch of the final layout for a single column ADC was just 22 μm as shown in Fig. 11. The first three blocks from the left and the 5-bit register to the right, accounting for 51% of the area, were dedicated to subrange selection and overlapping subrange creation. The remaining circuit is the 5-bit SAR ADC.

Fig.11 The distribution of function blocks inside each column ADC indicates that 51% area is used for subrange selection and overlapping subrange creation. The 5-bit DAC occupies 22 μm by 307 μm and is 20% the total area. It is only 3% of a conventional binary weighted 9-bit DAC.

The circuit was fabricated at TSMC in their 0.35 μm 2P4M high-voltage process. A die photo of the fabricated chip is shown in Fig. 12. The entire chip measures 2.4 mm by 2 mm and contains a number of test circuits. It includes 45 ADC channels, each 22 μm by 1570 μm . An analog multiplexer switch allows testing of each ADC individually. Instead of using off-chip field-programmable gate array (FPGA) for

digital timing control, the chip was integrated with a global control logic measuring 330 μm by 125 μm to synthesize all timing signals. The globally shared 4-bit resistor ladder was built from 32 identical 867 Ω unity resistors (double-poly resistor), each measured 100 μm by 6 μm , in a common-centroid layout with a total area of 300 μm by 130 μm . Dummy resistors identical to the unit resistor are placed at the exterior to improve the matching.

Fig. 12 The proposed CPOSSAR ADC was fabricated in TSMC's 0.35 μm 2P4M high voltage process. The die photo shows the 45 ADC channels that share the same resistor ladder bias and the digital control logic.

Post-layout simulation was performed using a simulation test-bench involving only one column ADC. The layout of a single column ADC, the zero-offset buffer bank, and the 4-bit resistor ladder were extracted from the physical layout to generate the netlist containing parasitics. The post-layout simulation was performed with a 3.3V power supply at the sampling rate of 1 MS/s when a 16.6 kHz sinusoidal wave input with 1090 mV_{pp} and 1.7145 V offset was provided. A 1.05 ms simulation was executed and it returned 1024 digitized values. This digital output was processed in MATLAB to plot the FFT spectrum and calculate SNR, SINAD, SFDR and ENOB. As is shown in Fig. 13, The SINAD achieved 55 dB, providing an ENOB of 8.8 bits based on equation (6).

$$ENOB = \frac{SINAD - 1.76}{6.02} \quad (6)$$

The CPOSSAR ADC was post-layout simulated when applying a 16.6 kHz sinusoidal wave with 1090 mV_{pp} and 1.7145 V offset at the sampling rate of 1 MS/s. 1024-point FFT was performed to calculate the SNR, SINAD, SFDR and ENOB.

4. Experimental Results

The fabricated CPOSSAR ADC was tested using two custom printed circuit boards. The main board communicated with a personal computer and generated bias signals. The second board held the device under test (DUT) and contained low-pass filters and buffers for the analog inputs. The two boards were then connected through board-to-board connectors to ease the replacement of the DUT. The DUT was powered by a 3.3 V analog power supply and a 3.3 V digital power supply separated on the main board.

4.1 Static performance measurements-Effectiveness of overlapping subrange assisted calibration.

The measurements started from the Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) tests based on the standard histogram method documented in IEEE std 1241-2010[13]. The overlapping subranges were initially disabled by setting the shifting voltage of the level shifter to 0 mV. After this base measurement the shifting voltage was adjusted to minimize the DNL and INL. In both measurements a 900 kHz external square wave was provided from an Agilent 32250A function generator for a 50 kS/s sampling rate. An 18.31 Hz sinusoidal wave with 1.054 V_{pp} and 1.672 V offset was provided from a Tetronix AFG 3252. A total number of 262144 samples were digitized to create the histogram and calculate DNL and INL.

The full conversion range is determined by the output swing of the level shifter and the transmission range of the NMOS in bias switch and capacitor DAC. They overlap between 1.15 V and 2.25 V based on a separate test circuits on the chip. In the subsequent test, the full reference scale was set to be from 1.16 V to 2.24 V.

The DNL and INL measurements results obtained without introducing the overlapping subranges are shown in Fig. 14. The maximum DNL was +5.14 and the minimum was -1. Many codes with -1 LSB DNL were missing codes. By observation, each cluster of missing codes is accompanied by a spike to the left with DNL error larger than +1. This pattern was the result of the mismatched DAC reference voltages that are higher than ideal values. The peak value of +5.14 LSB further quantifies the largest variation to be ~5 V_{LSB}, or ~10 mV. For INL result, the maximum of +5.35 and the minimum of -5.34 were observed.

Fig. 14 The maximum and minimum DNL of the CPOSSAR ADC was measured +5.15 and -1 when the overlapping subranges were not used. The corresponding maximum and minimum INL was +5.35 and -5.34.

The resistor ladder reference voltages, V_{capL} and V_{capH} , were then both adjusted upward by 10 mV to create the alignment pattern shown in Fig. 4. The shifting offset of the level shifter was made 32.5 mV to generate the overlapping subranges. When the data post-processing protocol described in Fig. 4 was implemented, the DNL and INL measurement results are shown in Fig. 15. 98% codes' DNL are distributed between ± 1 LSB and the peak for the rest is +1.27 LSB. No missing codes exist after the calibration. The INL was improved by more than 2 LSBs for both the maximum and the minimum. The INL of 3.2 is less important than DNL for imager sensor applications because of the noise and the non-linearity from the pixel sensor[14].

Fig. 15 The maximum and minimum DNL of the CPOSSAR ADC was improved to +1.27 and -0.92 LSBs when the overlapping subranges are used. The corresponding INL error was +3.17/-3.18 LSBs.

4.2 Dynamic performance measurements

The dynamic characteristics were measured by providing a sinusoidal signal with 1 V_{pp} amplitude and 1.672 V offset to the ADC at different sampling rates ranging from 1 kS/s to 1.1 MS/s. To ensure coherent sampling for the FFT analysis the input frequency was increased accordingly, such that 233 cycles of the sinusoidal wave were recorded with 4096 samples. The 4096-point FFT spectrum was then plotted at each sampling rate to calculate SNR, SINAD, SFDR, and ENOB. Fig. 16 shows the FFT spectrum when the conversion rate was 1.1 MS/s. Due to the relatively large non-linearity presented in the INL measurement, the ENOB of the ADC dropped by 3-bits from its post-layout simulation result.

Fig. 16 The 4096-point FFT spectrum of the fabricated ADC was obtained by providing a 62.57 kHz sinusoidal wave with 1 V_{pp} and

1.672 V offset at the sampling rate of 1.1 MS/s.

The ENOB and SFDR at different sampling rate are plotted in Fig. 17. These two dynamic characteristics remains stable for low sampling rate, and dropped dramatically after the sampling rate went over 1.1 MS/s.

Fig. 17 The CPOSSAR ADC was tested at various sampling rate with a 1 Vpp and 1.672 V offset sinusoidal wave. Its ENOB and SFDR are plotted across the tested sampling rate.

To better analyze the non-linear nature of the fabricated ADCs, the transfer function of the 5-bit capacitor array was measured to justify its sufficient linearity. A series of evenly spaced DC voltages was created by a Keithley 2401 SourceMeter. These voltage signals were low-pass filtered with an R-C filter with 33.9 kHz bandwidth and digitizing by the ADC with 10000 samples/step. The transfer function of the averaged data was plotted using only the 5-bit coarse conversion result. Fig. 18(A) shows the measured transfer function versus the ideal case. It was then used to calculate the DNL and INL, as shown in Fig. 18(B) and (C). Both DNL and INL confirm that a 7-bit ratio-accuracy was achieved by the 5-bit capacitor array.

Fig. 18(A) The transfer function of the 5-bit capacitor array was measured. (B) The DNL was derived from the measured transfer function and (C) the INL was derived from the DNL, both showing that the 5-bit component achieved 7-bit ratio-accuracy.

Since the fundamental non-linearity source of the proposed ADC is not the mismatch of the capacitor, other reasons are proposed and will be taken care of in the future work. The first reason is the insufficient reference voltages decoupling inside the chip due to the lack of on-chip capacitors. The second reason is the digital noise coupling through substrate and between columns that can not be captured by simulating a single channel. The third reason is the process variation induced mismatch between dummy switches and main switches in level shifters that were not evaluated in post-layout simulation. The mismatched devices create non-ideal overlapping subranges due to input dependent charge injection.

4.3 Power

The proposed CPOSSAR ADC utilizes more continuous-time analog circuits for sampling, reference buffering, subrange selection, and shifting than conventional SAR ADCs, therefore it consumes more static power for biasing. In idle state, a total of 64 mW was measured at 3.3 V power supply. 17 mW was consumed by the global reference buffers. The rest 47 mW is evenly distributed in 45 columns,

resulting in 1 mW/column static power. The dynamic power at 1 MS/s was 14.5 mW. 25% of the power was consumed by the digital control logic shared by all columns. The remaining 75% was evenly consumed by 45 channels, resulting in 242 μ W/column dynamic power.

4.4 Performance summary and comparison

The proposed CPOSSAR ADCs achieved 9-bit quantization resolution with the maximum sampling rate of 1.1 MS/s. Under the 3.3 V power supply, they consume 1 mW/column static power and 0.2 mW/column dynamic power at 1 MS/s. One ADC channel occupies 0.035 mm² in TSMC's 0.35 μ m 2P4M high-voltage process.

Table I summarizes the performance of this work and other related works used in CMOS imager sensors. Multiple-ramp Single-slope (MRSS) and 2-step Single-slope (2-step SS) ADCs feature in small channel area and low power[1], [2]; SAR ADCs are highly power efficient[14]; Cyclic ADCs perform high-resolution at fast conversion speed[15]. To assist a uniform comparison across different topologies, the throughput per unit time per unit chip area in bits ($Mbit / (s \cdot mm^2)$) for each reported ADC is measured. The figure of merit (FOM) based on this definition can be expressed as

$$FOM = \frac{N \times f_s \times K^2}{A} \quad (7)$$

where N is the resolution, f_s is the conversion rate, A is the channel area, and K numerically equals to the minimum gate length to account for technology differences. A higher value of FOM corresponds to the more efficient utility of silicon area to achieve a specific data conversion throughput. A similar FOM was used to evaluate the area efficiency improvement of several small ADCs with time-interleaved sampling over a single ADC operating at much higher sampling rate [16]. It is written as

$$FOM = \frac{f_s}{A} \quad (8)$$

Column-parallel ADCs used in CMOS image sensor are space-interleaved data converters very close to the time-interleaved platform. Because the pitch size and channel area is highly constrained for column-parallel ADCs, their area efficiency in high throughput and high resolution imager sensor array are significantly important. So the FOM in (7) is proposed by adopting (8) and introducing the resolution (N) and the technology scaling factor (K). The proposed FOM scales linearly with N because the conversion rate, f_s , for SAR, Cyclic, and CPOSSAR ADCs decreases linearly with each additional bit. The conversion rate for MRSS and 2-step SS follows a semi-linear semi-exponential relation with N . The same FOM is simply used because the nominator remains relatively unchanged when adjusting the performance.

The resultant FOM values for all ADCs indicate that the CPOSSAR ADCs exhibit higher area efficiency ($\times 4, \times 2, \times 2.5$) than MRSS, SAR, and Cyclic ADCs, but are not as efficient as the 2-step SS ADCs. However, the conversion speed of the 2-step SS ADCs is limited under 1 MSPS. They require $(2^M + 2^N)$ clock cycles for an $(M+N)$ bits conversion. But only $\sim (M+N)$ clock cycles are required by the

CPOSSAR ADCs. This makes the CPOSSAR ADCs scale better than 2-step SS ADCs.

Table I also listed the minimum element matching requirement for SAR, Cyclic, and CPOSSAR ADCs. Capacitors in N-bit SAR and Cyclic ADCs should be no less than N-bit ratio-accurate. But based on the analysis in section 2.2, CPOSSAR ADCs require only $(N+1)/2$ bits ratio-accurate capacitors, improving the capacitor mismatch tolerance significantly.

Table. I. The performance comparison with other imager ADCs

	Snoeij, 07 [1]	Lim, 09 [2]	Matsuo, 09 [14]	Furuta, 07 [15]	This work
Technology (μm)	0.25	0.35	0.18	0.25	0.35
Topology	MRSS	2-step SS	SAR	Cyclic	Sub-ranging
ADC Pitch Size (μm)	7.4	5.6	4.2	40	22
Resolution (bits)	10	10	12/14	12	9
Supply Voltage (V)	2.5/3.3	2.8	1.8/3.3	2.5/3.3	3.3
Conversion time (μs)	16	4	1.7	0.5	0.71
Input range (V)	1	N/A	N/A	2	1.1
DNL (LSB)	N/A	+0.53/-0.78	+0.7/-0.42	+0.76/-0.81	+1.27/-0.92
INL (LSB)	+1.2/-1	+1.42/-1.61	+2/-15	+20.6/-2.25	+3.17/-3.18
Power/column (mW)	0.11	0.11	0.041	0.43 (@3.3V)	1.2
Area (mm^2)	0.004	0.003	0.011	0.088	0.035
FOM ($M\text{bits} / (s \cdot \text{mm}^2)$)	10	102	21	17	44
Min cap accuracy (bits)	N/A	N/A	= resolution	= resolution	(resolution+1)/2

5. Conclusion and future work

A 22 μm -pitch 9-bit column-parallel overlapping sub-range SAR ADCs architecture was proposed and fabricated for CMOS pixel sensor. A conventional 5-bit SAR ADC is reused twice to improve the quantization resolution from 5 bits to 9 bits. The low resolution ADC reduced the DAC capacitance to only 3% that of a traditional binary weighted 9-bit SAR ADC. An overlapping subrange conversion was implemented. It reduced the accuracy requirement of quantization elements in each channel from 9 bits to 5 bits. The proposed method significantly improved the maximum DNL from +5.14 to +1.27, removed all missing codes, and reduced the INL error by over 2 LSBs. The throughput in bits per unit time per unit chip area is a factor of 4, 2, and 2.5 higher than MRSS, SAR, and Cyclic ADCs. At last, the relatively large power consumption per channel of the proposed CPOSSAR ADCs can be improved by removing sampling amplifier and implementing all digital comparator circuits.

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