Surfaces and interfaces governing the OMVPE growth of APD-free GaP on AsH₃-cleaned vicinal Si(100)

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Abstract

Direct growth of GaP on Si enables the integration of III-V and Si optoelectronic devices for a wide variety of applications, and has therefore been the subject of much research for many decades. Most of this effort has been directed toward overcoming the two main technical challenges: 1) removing atmospheric oxygen and carbon contamination and 2) establishing the conditions needed for "APD-free" III-V epitaxy (i.e., without antiphase domains). We have developed an OMVPE process for APD-free GaP growth on Si which overcomes both challenges by using AsH₃ to clean and prepare the Si surface *in situ* at a relatively low temperature. This process is based upon a very brief "AsH₃-cleaning" step which simultaneously removes atmospheric contamination (thereby eliminating the need for Si regrowth) and creates a single-domain As-terminated Si surface. Here we discuss the key process steps using results from a suite of analysis tools.

Keywords: B2. Semiconducting silicon; B2. Semiconducting III–V materials; A3. Organometallic vapor phase epitaxy; A1. Surface structure; A1. Nucleation; B3. Solar cells

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1. Introduction

The growth of GaP on Si is a classic polar/non-polar heteroepitaxial system in which the structure of the initial Si surface can be altered to change the properties of the subsequently grown GaP [1],[2]. In particular, single-monolayer steps on the Si surface can create undesirable antiphase domains (APDs) in the GaP, so the creation of an oxide-free bilayer-stepped "single-domain" Si surface prior to GaP nucleation has been deemed essential [3-6]. The process described here uses an HF-dip followed by AsH₃ exposure to create a clean, single-domain vicinal As/Si(100) 1x2 surface, and the resulting GaP epilayer is APD-free. Because this is a relatively fast, single-chamber process, it offers a potentially elegant method for integrating III-V and Si materials. In this paper, we will focus on various process details which may affect the quality of the resulting GaP epilayer.

2. Materials and Methods

Si(100) substrates with a 4° offcut toward (111) were used in this study, but single-domain As/Si surfaces were also obtained for 2° and 6° offcut angles. These samples were cleaned with a 2:1:10 NH₄OH:H₂O₂:H₂O mixture and rinsed in H₂O. Next, a H-terminated surface was formed by a 30 sec dip in 10% HF followed by a brief (<10 sec) dip in DI H₂O.

Samples were then loaded into a low-pressure (50 torr) OMVPE chamber supplied with AsH₃, PH₃ and triethylgallium (TEG) carried by flowing H₂. They were first heated (with a 5 min ramp time) to ~800°C under ~0.03 torr AsH₃, then immediately cooled to ~700°C for GaP nucleation

and growth. The AsH₃ exposure removes surface contamination and creates a clean, bilayer-stepped As/Si 1x2 surface (Fig. 1a). Throughout this treatment, the Si surface structure is monitored with *in situ* reflectance-difference spectroscopy (RDS).

Samples were then cooled to near room temperature (under either AsH₃ for As/Si samples or PH₃ for GaP/Si samples) before transfer under vacuum to a UHV surface-analysis chamber for low-energy electron diffraction (LEED), Auger electron spectroscopy (AES), and scanning tunneling microscopy (STM). Additional experimental details can be found in Refs. [7] and [8].

3. Results

An examination of our pre-nucleation surfaces with LEED indicates that the resulting As/Si surfaces are indeed single-domain, with dimer rows parallel to the surface steps (Fig. 1a). These surfaces were free of C and O to within the detection limits of AES (3 to 5% coverage), though some trace amounts may remain.

Although LEED provides no information about the structure of the interface, it does indicate that the GaP epilayer orientation is consistent with the {Si, V, Ga, P} stacking sequence established by the As/Si surface (Fig. 1b). The GaP epilayer is free of anti-phase domains (APDs), as evidenced by both plan-view and cross-sectional transmission electron microscopy (TEM) in Fig. 2.

The basic process steps and results have already been discussed elsewhere (Refs. [7] and [8]). The remainder of

this paper will focus instead on process details which can affect the quality of the resulting GaP/Si.

3.1 Surface structure

The first and most important consideration for achieving APD-free heteroepitaxy is the structure of the As/Si surface. Under the conditions described, in our OMVPE reactor, the resulting surface is As/Si 1x2. Preliminary *ab initio* calculations for this surface indicate the 1x2 surface is stabilized by anisotropic stresses generated by As-As dimers. However, beyond this, the situation becomes much more complicated.

One complication arises from small-scale differences in surface structure and composition as the AsH₃-exposure conditions are changed. A careful re-examination of (unpublished) post-run room-temperature STM images taken during an earlier study revealed two examples of this: 1) The As coverage at 700°C was saturated at 1 ML, while at 800°C many dimers are asymmetric, consistent with incomplete As coverage (based on the appearance of dimers in STM images). 2) At 700°C the step edges adopt a strain-stabilized "5-7-5" reconstruction [9]; step edges at 800°C do not, consistent with the lower surface stress expected for incomplete As coverage.

AsH₃ etching of the Si substrate via the formation of volatile SiH₄ [10] can also create a wide range of surface morphologies, which are dependent upon the AsH₃ partial pressure, etching time, and sample history. For example, prolonged etching under ~0.03 torr AsH₃ tends to generate a mixed 1x2/2x1 surface with single steps, whereas increasing the AsH₃ partial pressure to ~1 torr quickly roughens the surface [10].

Furthermore, these changes all require mass transport of *subsurface* Si (the surface layer is As), and this can slow these transitions to a time scale of minutes. This time sensitivity adds yet another dimension to the surface-structure phase space. Finally, the use of different sample holders with differing thermal properties can introduce additional confounding factors.

Because the surface structure is complex and very sensitive to process conditions, *in situ* RDS is an invaluable tool for process development. It is sensitive to surface anisotropy, and, when combined with LEED or other surface probes, can be used to detect the formation of As-As dimers on the Si surface, and monitor the ratio of 1x2 to 2x1 domains.

In Fig. 3, a sample is heated under AsH₃ until the RD signal at the two selected photon energies differs, indicating the formation of an anisotropic surface. This provides an *in situ* indication that the temperature needed to form the surface needed for GaP nucleation is reached, but not greatly exceeded, minimizing the thermal load and associated damage to any devices in the underlying Si. If reactor conditions change (i.e. the sample temperature calibration changes), then RDS can be used to re-establish the proper conditions.

3.2 Etch-related Si "spikes"

Atomic H released from AsH₃ decomposition at the surface removes C and O from the surface, presumably by forming volatile species such as CH₄ and H₂O [10]. However, this cleaning may leave some remnants at concentrations below the detection limit of AES.

Atomic-force microscope (AFM) images of AsH₃-etched Si surfaces often exhibit Si spikes (Fig. 4a), and the height of these spikes correlates with AsH₃ partial pressure and exposure time. The most logical explanation for this is that AsH₃-etching of the Si is locally impeded by small remnants of etch-resistant surface contamination (Si-C bonds, for example).

Because the areal density of these spikes is very low, most of the resulting As/Si surface and subsequent GaP/Si is flawless. However, plan-view TEM images of subsequently grown GaP/Si often contain small strain contrast features, possibly arising from the presence of small, coherently strained precipitates or dislocation loops, with a similar areal density (Fig. 4b). The exact identity and impact of these small strained defects are not yet known. If they are indeed harmful, then our results suggest that efforts to eliminate them should be focused on better environmental control of extrinsic contamination of the Si surface during and after the wet chemical cleaning.

3.3 Faceting of the GaP surface

The plan view TEM images in this paper clearly demonstrate that smooth surfaces with only a small amount of rippling can be grown with this process. However, the same growth recipe sometimes produces (100) faceted regions (Fig. 5a). A myriad of factors could be inducing this faceting and the exact cause is not known. Nonetheless, it may be useful to discuss a possible link to surface contamination – namely, that surface contamination could be stabilizing (100) surface facets.

First, it is important to note that our system has the cleanliness needed to prepare and observe clean phosphide (100) surfaces [11], as evidenced by the GaP(100) 2x2/c(4x2) surface reconstruction in Fig. 5b. Although our LEED patterns for clean GaP(100) surfaces show nice long-range order, the corresponding STM images (taken during a prior study) contain many defects and considerable small-scale disorder.

It would be logical to assume that contaminated surfaces are far more defective, but for some types of contamination this is not the case. Our STM images from a previous study of GaP(100) surfaces intentionally contaminated with impurities from the set {C, Si, Ge, In, As} show that the surface can adopt a nearly flawless "3x1" reconstruction (Fig. 5c). Furthermore, and most importantly for this discussion, they appear to be very stable, as evidenced by the fact that they remain nearly flawless and easy to image with STM (under UHV) for days.

If this type of "3x1" surface only occurred occasionally, it could perhaps be ignored. But we have found that it forms

quite readily in the presence of a variety of impurities from the set {C, Si, Ge, In, As}. We therefore suggest that faceting of vicinal GaP(100) might be induced by contamination from this set of elements.

3.4 Dislocation glide

TEM images of GaP films exceeding the Matthews-Blakeslee critical thickness [12] contain very widely spaced misfit dislocations (Fig. 6a) resulting from the glide of threading dislocations. However, the misfit dislocation density is very low, and XRD shows very little relaxation. This implies that only the extremely low dislocation density threading up from the Si substrate is available for the initial strain relaxation, and very few (if any) new dislocation half loops have nucleated at the GaP growth surface. This metastable situation does not persist for thicker (0.5 μm) GaP layers, for which significant relaxation is observed.

3.5 Incorporation of arsenic

The LEED images in Fig. 1 indicate that the GaP epilayer orientation is consistent with the {Si, V, Ga, P} stacking sequence established by the initial As/Si surface. They do not, however, provide any information about the elemental composition of the GaP/Si interface. At a GaP growth temperature of 700°C, interfacial intermixing and other forms of mass transfer are quite likely. For this reason, the GaP/Si interfacial layer in the Fig. 1b schematic is simply labeled "Group V". (The interface properties of GaP/Si grown at a much lower temperature using tertiarybutylphosphine [13] could be quite different.)

If the As layer remained statically at the GaP/Si interface, it should be readily visible in the SIMS profile in Fig. 6b. It is not, so the As layer must be somehow displaced during the growth of the GaP epilayer. Furthermore, the As concentration throughout the 0.5 μm GaP epilayer in Fig. 6b remains nearly constant, suggesting that it is the result of background As_x in the growth chamber (and not simply diffusion or migration of the original interfacial As).

4. Summary

A quick, single-chamber process has been developed to produce a single-domain As/Si 1x2 surface, which in turn serves as the template for APD-free GaP. In this process, a vicinal Si(100) substrate is dipped in 10% HF and then briefly exposed to ~0.03 torr AsH₃, first at ~800°C, then at ~700°C before GaP growth. Process details which might

affect the quality of the resulting GaP epilayer were discussed using results from a suite of analysis tools.

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Figure 1. Schematic diagrams and 100-eV LEED images for (a) an As/Si 1x2 surface [sample number PD299] and (b) a GaP/Si epilayer. In (b), the LEED pattern is for a ~75 nm GaP/Si epilayer which was grown [PD305], exposed to air, and then re-annealed under PH_3 [PD308]. (The air exposure damaged the surface such that only a trace of the expected $2\times 2/c(2\times 4)$ reconstruction from surface H is observed.) Both LEED images indicate 1x2 surfaces with surface dimer rows parallel to the step edges, and the "step-splitting" in (a) indicates a double-stepped surface. Single-domain As/Si 1x2 LEED patterns were also obtained for 2° and 6° offcut samples [PD214, PD232]. They are nearly identical to (a) in appearance, aside from the offcut-dependent step-splitting.

Figure 2. (a) High-resolution lattice TEM image of GaP/Si showing excellent crystallinity of both the GaP epilayer and interface [PD288]. (b) Plan-view TEM image of ~96 nm GaP/Si [PD341]. No APDs are visible. Similar APD-free images were obtained over multiple images totaling $160\ \mu\text{m}^2$. (c) Cross-sectional image of GaP/Si [PD288]. No APDs are visible at the interface.

Figure 3. RD signal at two different photon energies plotted as a function of time. The sample [PD341] was initially heated under AsH_3 , then cooled slightly for GaP growth (to the right of the vertical line). $T_{\text{sample holder}}$ (the backside of the sample holder, monitored with an optical pyrometer) was slightly hotter than the sample.

Figure 4. (a) AFM image of AsH_3 -etched Si [PD327]. Image size is $2\ \mu\text{m} \times 2\ \mu\text{m}$. The height of the Si "spikes" on this surface (circled) is $\sim 4\ \text{nm}$. The height of the spikes is related to the AsH_3 -etching time and conditions. Inset: Proposed mechanism for spike formation, (b) Plan view TEM image of $\sim 96\ \text{nm}$ GaP grown on an " AsH_3 -cleaned" Si surface [PD341]. A possible link between the small defects (four encircled) and the Si spikes in (a) is discussed in the text.

Figure 5. (a) SEM image of ~ 75 nm GaP/Si showing a faceted region seen on some samples [PD305]. Side view: AFM images indicate that the triangular regions in the SEM image are (100) facets. (b) STM and (inset) 30-eV LEED image for a clean GaP(100) surface exhibiting a $2\times 2/c(4\times 2)$ surface reconstruction. STM image is $200 \text{ \AA} \times 200 \text{ \AA}$ [PB596]. (c) GaP(100) surfaces contaminated with {C, Si, Ge, In and/or As} tend to adopt a " 3×1 " surface reconstruction. STM image is $1000 \text{ \AA} \times 1000 \text{ \AA}$ [PB982]. A possible link between the faceting in (a) and the " 3×1 "-stabilized surface in (c) is discussed in the text.

Figure 6. (a) Plan view TEM of ~ 96 nm GaP/Si containing a single (cross-slipped) misfit dislocation [PD341]. (b) A SIMS depth profile for $\sim 0.5 \text{ }\mu\text{m}$ GaP/Si, taken by sputtering with Cs^+ and analyzing negative secondary ions under high mass resolution [PD356]. There does not appear to be an As monolayer at the GaP/Si interface.