Minority-carrier lifetime and defect content of *n*-type silicon grown by the noncontact crucible method

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Abstract: We evaluate minority-carrier lifetime and defect content of *n*-type photovoltaic silicon grown by the noncontact crucible method (NCC-Si). Although bulk impurity concentrations are measured by inductively coupled plasma mass spectroscopy to be less than one part per million, homogeneously throughout the as-grown material we observe lifetimes in the ~150 μ s range, well below the theoretical entitlement of single-crystalline silicon. These observations suggest the presence of homogeneously distributed recombination-active point defects. We compare an industry-standard gettering profile to an extended gettering profile tailored for chromium extraction, to elucidate potential gains and limitations of impurity gettering. Near the ingot top, gettering improves lifetimes to 750 and >1800 μ s for standard and extended profiles, respectively. Relatively lower gettered lifetimes are observed in wafers extracted from the ingot middle and bottom. In these regions, concentric-swirl patterns of low lifetime are revealed after gettering. We hypothesize that gettering removes a large fraction of fast-diffusing recombination-active impurities, while swirl microdefect regions reminiscent of Czochralski silicon can locally limit gettering efficiency and lifetime. Apart from these swirl microdefects, a low dislocation density of $<10^3 \text{ cm}^{-2}$ is observed. The millisecond lifetimes and low dislocation density suggest that, by applying appropriate bulk microdefect and impurity control during growth and/or gettering, *n*-type NCC-Si can readily support solar cells with efficiencies >23%.

Key words:

A1. Defects

A1. Impurities

A2. Top-seeded solution growth

B2. Semiconducting silicon

B3. Solar cells

1. Introduction

Dislocations [1, 2] and metal impurities [3, 4] have historically been two of the most ubiquitous lifetime-limiting defects in crystalline silicon for photovoltaics. As impurity-management techniques evolve [5-7], extended defects become increasingly important in limiting the bulk minority-carrier lifetime. Thus, emphasis is placed on growth of crystals with low dislocation density (below $\sim 10^4 \text{ cm}^{-2}$), including Czochralski silicon (CZ-Si), kerfless epitaxial silicon [8], small-grained multicrystalline silicon [9], and a novel technique known as the noncontact crucible method.

The NCC-Si method is an emerging technique for growing high-quality silicon ingots for photovoltaic (PV) applications [10-14]. The method which is similar to the Kyropoulos technique developed in 1926 [15] and widely used for growth of large single crystals of alkali halides such as sodium chloride and oxides such as sapphire [15-17], leverages cheaper traditional crucible multicrystalline silicon (mc-Si) and dislocation-free CZ-Si ingot manufacturing techniques to achieve a single-crystalline silicon ingot with low ($< 10^4 \text{ cm}^{-2}$ [14]) dislocation density. In conventional mc-Si growth [18-20], solidification starts from the crucible bottom, where high thermal and mechanical stress causes plastic deformation. The resulting crystal contains a variety of defects, including grain boundaries, stacking faults and dislocations, which can be in average densities as high as 10^6 cm^{-2} [18, 21]. In addition, the concentration of in-diffused impurities is high [22] (up to 10^{15} cm^{-3} for the case of iron [23, 24]), as the crucible is in direct contact with solidified silicon from the onset of crystallization. On the other hand, solidification in the NCC-Si method starts from the top, using a CZ-Si-like seeding and necking process. Crystallization therefore proceeds outward from the top-center of the melt (Figure 1), avoiding contact between the crucible and the growing ingot. As crucible wall nucleation and

contact are minimized, so too is the dislocation density [25] and impurity content [26, 27]. However, as-grown lifetimes for the NCC-Si are reported to be 118 μs maximum [11], well below the millisecond range entitled by a low dislocation density of $<10^4 \text{ cm}^{-2}$.

In this contribution, we examine the defect content of NCC-Si and explore the extent to which as-grown lifetimes are limited by fast-diffusing impurities that can be mitigated by gettering. We demonstrate the potential of phosphorus diffusion gettering to improve the bulk minority-carrier lifetime to levels as high as 1.8 ms. From this experimental observation, we conclude that the as-grown lifetime is limited by a combination of “getterable” impurities (*e.g.*, Cu, Ni, Fe, and/or Cr) [28-30]. In addition, in gettered material, we observe “defect striations” similar to swirl microdefect-rich regions in CZ-Si [31]. We speculate that the defects in the swirl-like regions hinder local gettering efficiency by acting as internal gettering sites [24, 32, 33].

2. Materials & Methods

For the material considered in this study, an ingot was grown using NCC-Si method at the Graduate School of Energy Science, Kyoto University, Japan. The ingot was a tapered cylinder, measuring 20.5 cm at its maximum diameter (**Figure 1**) and 6.2 cm in length, yielding a mass of 4.040 kg. A cylindrical crucible 26 cm in diameter was employed, with a Si melt depth of 5 cm. After the necking process, the ingot was grown by cooling the melt by $\Delta T_{\text{in}} = 28.9 \text{ K}$ without pulling, ΔT_{in} being the difference in temperature between the start of crystallization at the seed and the start of pulling. The ingot was then grown while pulling upward at a rate of 0.2–0.4 mm/min and cooling the melt by $\Delta T = 51.3 \text{ K}$, where ΔT is the temperature difference between the start and termination of crystallization. The diameter of the ingot decreased during pulling by a small cooling rate of 0.2 K/min.

Sample wafers (size 100 mm $\times$ 100 mm $\times$ 180 μm) were extracted from near the top, the middle and the bottom of the ingot height. Contrary to the industry-standard mc-Si ingot crystallization, in NCC-Si material, 100% ingot height (top) corresponds to the *first* part of the ingot to solidify, and 0% (bottom) the *last* (**Figure 1**). The resistivity of the samples was $\sim 1.0 \text{ }\Omega\text{-cm}$, $0.9 \text{ }\Omega\text{-cm}$ and $0.7 \text{ }\Omega\text{-cm}$ for the wafers from near the top, the middle and the bottom respectively.

As-grown unpassivated lifetimes were measured on full wafers, which were then laser-cut into smaller samples ($5 \times 3.5 \text{ cm}^2$) to accommodate the size limitation of our surface-passivation annealing furnace. The wafers were then etched to remove saw damage in a 4-min CP4 etch (removed $\sim 13 \text{ }\mu\text{m}$ on each side), RCA cleaned (without a final HF dip) and passivated for as-grown lifetime measurements. After as-grown lifetime measurements, samples were dipped in HF for removal of the passivation layer and cleaned in RCA in preparation for gettering.

Passivation involved formation of a 20 nm layer of Al_2O_3 deposited by atomic layer deposition at 200°C (Cambridge NanoTech Savannah 200) [34], followed by a 30 min anneal at 350°C in N_2 ambient. Gettering was performed by phosphorus in-diffusion in a POCl_3 tube furnace (Tystar Tytan 3800), using either an industrial standard (STD) process or an extended (EXT) process. The STD process includes loading the sample at 700°C followed by a 25 minute plateau at 845°C , and unloading at 845°C . The EXT process consists of the same plateau at 845°C followed by a 2 hr anneal at 650°C before unloading. The EXT process was inspired by experience with the successful extraction of interstitial iron from *p*-type materials [35, 36], but tuned for the extraction of chromium following the guidance of reference [37]. Iron point defects are not expected to significantly reduce lifetime in *n*-type silicon, while chromium point defects are expected to remain recombination active in *n*-type silicon, because of the ratio of hole and electron capture cross sections [4].

Gettered wafers were then passivated following the procedure described above, after removing the n^+ region with a 2-min CP4-etch (removed $\sim 5 \text{ }\mu\text{m}$ on each side). Lifetime measurements were conducted using quasi-steady-state photoconductance decay and transient photoconductance decay (QSSPC, Sinton WCT-120) and microwave photoconductance decay (μ -PCD, Semilab WT2000).

For direct impurity measurements, two techniques were applied: inductively coupled plasma mass spectroscopy (ICP-MS), and synchrotron-based X-ray fluorescence microscopy (μ -XRF). The latter was performed at the Advanced Photon Source at Argonne National Laboratory, at Beamline 2-ID-D, with 10 keV incident X-rays, a spot size of $\sim 200 \text{ nm}$ full width at half maximum, and a step size of 220 nm.

Defect etching was used to reveal dislocations and bulk microdefects. To avoid toxic chromate-based etchants for environmental and personal safety concerns, the MIT laboratory uses the Sopori etch [38], a mixture of HF, CH₃COOH, and HNO₃ in a volume ratio of 36-15-2. Although the community lacks extensive experience with the Sopori etch to differentiate between surface features indicating intrinsic point defects and related defect complexes, it is possible to identify the presence of bulk microdefects in general using this technique.

3. Results

From a similar but earlier-grown *n*-type ingot, ICP-MS revealed as high as 0.08 parts per million by weight (ppmw) Cu and 0.09 ppmw Al in as-grown samples. Elements Fe, Ni, and Ti were below detection limits (<0.05 ppmw).

Synchrotron-based μ -XRF was not able to detect impurity-rich precipitates. Two samples were analyzed: as-grown and standard-gettered material from the middle height of the ingot. $\sim 20 \times 20 \mu\text{m}^2$ maps were obtained for both samples around defects revealed by etching.

Figure 2 shows lifetime maps before and after processing. As grown unpassivated lifetimes were low ($\sim 3 \mu\text{s}$), and striations appeared in the μ -PCD lifetime maps (**Figure 2(a - c)**). After passivation, lifetimes $> 150 \mu\text{s}$ were measured at an injection level of 10^{15} cm^{-3} . The distribution of as-grown-passivated lifetime was relatively homogenous within samples and along the ingot height (**Figure 2(d - f)**).

Processed (gettered) lifetimes improved significantly, as shown in **Figure 3**. Maximum effective lifetimes of up to 791 and 1885 μs were achieved for the STD and EXT gettering profiles respectively, at an injection level of 10^{15} cm^{-3} . In the top wafer, where the maximum gettered lifetime was obtained (**Figure 3a**), the lifetime distribution was relatively homogeneous (**Figure 2g**), and striations did not appear to have a significant impact on the gettered lifetime.

In the top wafer, the effective lifetime after the extended gettering process was more than twice the lifetime after applying a standard profile. In comparison, there was no significant

improvement by extended gettering in wafers from the middle and bottom positions of the ingot. The effective lifetime in wafers M1 in **Figure 3(b)**, B1 and B4 in **Figure 3(c)**, which are gettered by the extended process, are actually lower than those in equivalent positions, *i.e.* position M3, B3 and B2 respectively (see **Figure 2**), which are gettered by the standard process. Regions of low-lifetime and generally significant intra-wafer lifetime variation are observed in both standard and extended processes. The low lifetime regions appear to correspond to striations observed in the as-grown lifetime maps.

Figure 4(a) shows a lifetime map of sample M3. **Region A** corresponds to the middle of the full wafer shown in **Figure 2(b)**. It is observed that lifetime deteriorates progressively outwards from the center, with a distribution, which follows well-defined contours. The distribution of structural defects appears to follow a similar pattern as shown in optical microscope images, (**Figure 4b**) after the sample was defect-etched in Sopori. The center (**Region A**) and the periphery of the wafer (**Region E**) were mostly free from structural defects (with densities $<10^3 \text{ cm}^{-2}$)

4. Discussion

We assess the current lifetime “ceiling” and future lifetime entitlement of NCC-Si material, considering measured and inferred defect densities reported in this study.

Impurity concentrations are at or below the detection limit of ICP-MS and synchrotron-based μ -XRF, yet as-grown lifetimes are low ($\sim 150 \text{ }\mu\text{s}$), which suggests the presence of homogeneously distributed lifetime-limiting defects. The lifetime improvement achieved *via* gettering, especially the extended gettering process optimized for chromium, demonstrates that the lifetime-limiting defects are most likely getterable metal-impurities. It is plausible that chromium point defects are largely responsible for the initially low lifetime and dramatic lifetime improvement. Chromium is known to be recombination-active in *n*-type silicon [4] and has sufficient diffusivity and solubility to be gettered [37]. We acknowledge the possibility that small copper-, nickel-, and/or iron-silicide precipitates may also contribute, because despite low recombination activity of isolated point defects in *n*-type silicon, these species readily form recombination-active precipitates [39] but respond well to extended gettering [40-42].

For material extracted from the middle and bottom of the ingot, lifetimes were significantly lower and spatially inhomogeneous after gettering. Given that the ingot top (first to solidify) provides the highest-lifetime material, we acknowledge the possibility of an impurity that segregates during growth (but cannot be easily gettered) may limit lifetime in the middle and bottom wafers. However, the swirl pattern in the lifetime maps (**Figure 4a**) appears to correlate with the bulk microdefects (**Figure 4b**), suggesting the underlying cause for gettered lifetime suppression. The defect pattern appears to be similar to swirl microdefect regions [31, 43] found in single-crystalline silicon grown by the CZ or float zone methods. Swirl micro defect regions are associated with point-defect clusters - voids, stacking faults, and dislocation loops [44], which are favorable nucleation sites for metal-impurity precipitation. A mechanism where the defects act as efficient internal gettering sites for impurities [45], which later act as sources of contamination [41], may explain the comparatively lower gettering efficacy in these regions.

The 1.8 ms bulk lifetime achieved by extended gettering is sufficient to surpass 23% device efficiencies [8, 46]. The realization of high bulk lifetimes in NCC-Si material with extended gettering suggests that if more stringent impurity controls are implemented during growth, NCC-Si material may have the potential to achieve millisecond as-grown lifetimes, enabling low-temperature cell fabrication processes. To achieve homogeneously high lifetimes throughout the entire ingot, the swirl microdefects must be suppressed, especially in the lower parts of the ingot. Techniques employed to reduce bulk microdefect densities in CZ-Si may inspire approaches to reduce or eliminate this defect in NCC-Si material.

5. Conclusions

We evaluated the lifetime potential and defect content of PV silicon grown by the noncontact crucible method. Near the ingot top, minority-carrier lifetimes improved from 150 μ s to 1.8 ms after extended gettering, suggesting the presence of medium - or fast-diffusing metal impurities (*e.g.*, chromium). In the middle and bottom parts of the ingot, current gettered lifetimes are overall lower, more inhomogeneous, and follow a structural defect pattern revealed by defect etching). We suspect that the defects hamper the gettering efficiency, by acting as internal

gettering sites. The resemblance of the defect structure to the swirl microdefects observed in CZ-Si suggests that similar methods of bulk microdefect suppression may apply to NCC-Si material, enabling higher and more homogeneous lifetimes throughout the entire ingot. The potential to combine CZ-Si performance with mc-Si manufacturing costs indicates that NCC-Si has the potential to develop into a high-performance, low-cost, and readily manufacturable PV substrate.

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Figure Captions

Figure 1. Schematic of the NCC-Si growth method (not to scale). (a) A seed is inserted into the liquid silicon, followed by (b) necking to initiate crystal growth and crystallization inside the melt. (c) The final crystal avoids contact with the surrounding crucible walls. The ingot can be rectilinear or cylindrical, depending on crucible and heater configuration. Ingot top, middle, and bottom regions are indicated on the right.

Figure 2: Lifetime maps measured by μ -PCD. (a) - (c) as-grown unpassivated, full wafers. (e) - (f) as grown with passivation on 3.5cm x 3.5 cm wafers cut from respective positions in the full wafers. (g) - (i) processed (standard process in position 2 and 3 and extended process in position 1 and 4).

Figure 3: Effective minority-carrier lifetimes measured by QSSPC, after processing (standard process in position 2 and 3 and extended process in position 1 and 4).

Figure 4. (a) Lifetime map measured by μ PCD, and (b) light microscope image showing structural defect distribution in a sample from the ingot middle. Swirl patterns observed in lifetime maps coincide with bulk microdefects revealed by Sopori defect etching.

Figure 1

Figure 2

Figure 3

Figure 4