Micromachined Passive Phase-Change Cooler for Thermal Management of Chip-Level Electronics

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Abstract

This paper reports an efficient and reliable passive cooling device using phase-change of coolant in response to the needs of chip-level electronics applications in which heat dissipation must be removed as rapidly and continuously as possible. The design of this cooling device was developed with three functional layers including evaporator, wick, and reservoir, which provided enhanced capillary forces, allowing reliable cooling performance without wick dryout and coolant back flows. Cooling performance by the developed system was demonstrated experimentally with a combination of microfabrication techniques and nanomaterial synthesis, showing rapid and efficient heat removal ability by enhanced and extended capillary action during the operation. The chronic dryout limitation in micro cooling devices could be addressed by the proposed thermal system.

Keywords: *passive cooling, phase-change, chip-level electronics, coolant overflowing, microelectromechanical systems*

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1. Introduction

Effective thermal management for hot electronics is an essential issue for achieving a high-performance level of electronic devices without thermal damages including thermal shock, vibration, and degradation. Developments in semiconductor industries have allowed electron devices (chips) such as sensors, actuators, and transistors to be miniaturized to increase the manufacturing yield in a limited substrate. The decrease in the size of chips has led to increased heat dissipation per unit area of chip surface, while overall performance of chips has improved, and the cost of individual chips has been reduced [1-3]. Heat dissipation is considered to be a well-known reason for energy loss and a potential issue that may limit the device performance [2,3]. When these high heat fluxes exceed critical heat flux levels, which is the maximum heat flux that can be loaded on the chip and represents the operational limit of the device due to reduced heat transfer coefficients, the device temperature will be significantly increased, resulting in device failure [4,5]. Consequently, effective cooling of chip-level electronics is now becoming critical for next-generation electronics. To satisfy the rapidly increasing market demand for more compact, cost-effective, reliable, and faster cooling performance, new miniaturized active, passive, and hybrid cooling devices are being developed for many high-power density electronics applications.

The advent of microelectromechanical systems (MEMS) and nanotechnologies significantly impacted on the development of new microscale cooling devices, which are compatible with traditional semiconductor chips, to efficiently remove high heat flux from heat sources. Among various heat removal methods including active, passive, and a combination of both, passive cooling is now prevailing in current chip-level electronics applications because it does not require an additional power source that might need supporting electric circuit on the platform.

The main passive cooling systems use the basic heat transfer mechanisms including conduction [6,7], convection [8,9], and radiation [10,11] where the heat transfer rate generally relies on the thermal conductivity of substrate, properties of surrounding gases, or emissivity of solid surfaces. Such systems, however, are not suitable for many high-power density electronics because cooling efficiency highly depends on the material properties. Therefore, the combination of emerging MEMS technology and increasing demand for thermal management of chip-level electronics has led to the development of miniaturized two-phase cooling devices using superior heat absorption ability when the liquid coolants change to vapor [12-14], allowing the coolers to be used in a wide range of applications from ground to space environments [15-17]. In these systems, the microchannels have been fabricated by silicon (Si) etching technologies to use the capillary force of liquid coolants during the device operation. However, unexpected liquid-vapor interface oscillating [18], backward bubble flow [19], and dryout problems [20] occurred due to unstable capillary forces during the phase-change process, which have led to the development of continuous and reliable MEMS-based phase-change cooler to overcome dryout limitations.

In this paper, a micromachined passive phase-change cooling device was developed in response to the needs of chip-level electronics in which heat dissipation must be removed as rapidly as possible. The design of this cooling device was proposed with three functional layers (i.e., evaporator, wick, and reservoir layer), which provided enhanced capillary forces, allowing reliable cooling performance without wick dryout and coolant back flows. Cooling performance by the developed system was demonstrated experimentally with a combination of microfabrication techniques and nanomaterial synthesis, showing rapid and efficient heat removal ability by enhanced and extended capillary action during the operation. The chronic dryout limitation in micro cooling devices could be addressed by the proposed thermal system.

2. Design and theory

2.1. Device design

Fig. 1 depicts a schematic illustration of the proposed cooling device, composed of three main layers: evaporator, wick, and reservoir layer. The main cooling mechanism is to utilize phase-change of coolant, similar to the cooling process used in heat pipes. In conventional heat pipes, because the traveling vapor is in direct contact with turning liquid in the wick material, there is parasitic heat transfer from vapor to liquid during the circulation, which may cause oscillating vapor-liquid interface [18,19]. To prevent parasitic heat transfer, a physical (thermal) barrier (i.e., wick layer) between vapor and liquid channels was introduced in the proposed device. Therefore, the condensed liquid can continue to remove heat from the sources within a thermodynamically

Fig. 1. Three-dimensional schematic illustration (upper image) and cross-sectional view (lower image) of the three-layer stacked micromachined cooling device for chip-level electronics cooling.

stable state, which may maximize the efficiency of cooling performance. To prevent the back flows of both bubbles and condensed coolants, innovative structures were developed to feed the coolant continuously from the reservoir to the evaporator surface. Fig. 2 illustrates a schematic of designed and developed key structures in each layer. The evaporator layer which is in direct contact with hot chips is composed of three sections: an evaporator site, microchannels, and an intermediate chamber where condensed coolants are collected temporarily, as seen in Fig. 2a. The microchannels play a significant role in transporting condensed liquid coolant to the reservoir without external forces to prevent dryout. In the tapered microchannels, liquids can propel in the direction of lower pressure (i.e., narrower region) due to the differences in the axial pressure resulting from different curvatures (i.e., a narrower region has smaller curvature of the liquid) [21], forming a liquid meniscus along the wall with a contact angle. However, because the moving liquid meniscus is eventually pinned at the end of the channel without a sufficient force gradient [22,23], microstructures were introduced to break up the pinned meniscus at the end of channels, resulting in liquids overflowing into the intermediate chamber. The feeding of coolant from the reservoir to the evaporator surface is also limited by the capillary force. Although the condensed liquids return to the reservoir along the tapered channels and microstructures, liquid coolant must be pumped to the evaporator surface for continuous operation without dryout. In this study, the coherent Si wick, which consists of vertically aligned cylindrical micropore arrays and decorated nanowires, was fabricated to allow the pinned liquid meniscus at the end of pores to overflow out of the micropores so that coolant is able to remove the heat flux by touching the evaporator surface, as seen in Fig. 2b [24]. The reservoir layer includes three main sections: a coolant reservoir, microchannels, and an intermediate chamber, as seen in Fig. 2c. To collect the condensed liquids into the reservoir, the same design utilized for

the evaporator layer was adopted to the reservoir layer. Therefore, the wick dryout limitation can be dramatically prevented by a rapid refilling of coolant into the reservoir chamber.

Fig. 2. Schematic illustration of the design for (a) tapered channel and microstructure in evaporator layer, (b) coherent porous wick and nanowires in wick layer, and (c) tapered channel and microstructure in reservoir layer to allow liquid overflowing by the enhanced and extended capillary force, resulting in continuous coolant circulation.

2.2. Thermal resistance network

The heat transfer analysis of the proposed cooler begins from the junction of the chip loaded on a chip carrier, which serves for first-level cooling. Once the junction of the chip dissipates heat through the chip carrier, the heat transfers further across the layers of the cooler as second-level cooling, as seen in the cross-sectional scheme in Fig. 1. Fig 3a shows the MEMS chip mounted on a chip carrier where the lead frame was bonded to electrodes with gold bonding wires. As a first transport, the heat generated from the junction spreads throughout the Si chip and is transferred across the chip thickness using conduction. Considering a relatively small heat transfer area along the in-plane direction caused by the several-hundred-micron thickness of each layer of the cooler, the thermal resistance along the in-plane direction would be relatively larger than that along the cross-plane direction. For simplicity, it can be approximated as a one-dimensional conduction by employing a constriction thermal resistance to the network analysis [25,26]. The constriction thermal resistance for a junction diameter of d on the chip is given by:

$$R_c = \frac{1}{\sqrt{\pi dk}} \quad (1)$$

where k is the thermal conductivity of the chip material [25]. Therefore, the thermal resistance network for the chip combined with the developed cooler can be simplified as shown in Fig. 3b. As seen in the figure, the temperature of the evaporator layer is determined by the first chip package level's cooling, whereas the temperature of the reservoir is influenced by internal components in the cooling device, including coolant, nanowires, and porous Si wick. Considering the coolant/nanowires and coolant/porous Si wick can be approximated as parallel connections, the overall thermal resistance across the cooler layers is expressed by:

$$R_{cooler} = R_{evap} + \frac{1}{1/R_{cool-NWs} + 1/R_{NWs}} + \frac{1}{1/R_{cool-PSi} + 1/R_{PSi}} + R_{cool-res} \quad (2)$$

Fig. 3. (a) Image of the MEMS chip packaged on a chip carrier for first-level cooling and (b) thermal resistance network of a combination of a chip carrier and cooling device for simultaneous cooling. Scale bar: (a) 5 mm.

where $R_i = L_i/k_i A_i$. Subscripts NWs and PSi represent to the nanowires and porous Si, respectively. Note that the coolant was also considered as a conductive solid medium with a specific thermal conductivity because free and forced convection arising from the liquid movement can be negligible due to a small enough micron gap between each layer. In the following subsections, the thermal conductivities of each layer in the cooling devices will be theoretically estimated by the kinetic theory for thermal resistance network analysis.

2.2.1. Thermal conductivity of evaporator and reservoir layer

In micro- or nanoscale domains where the characteristic length L is comparable or smaller than the mean free path Λ , traditional macroscopic averaging heat conduction equation (i.e., Fourier's law) may no longer represent the motion of heat carriers because the heat flow in such domains is impeded by numerous collisions between heat carriers and boundary of the medium, impurities, or another wavepacket, resulting in “*classical size effect*” [27,28]. Consequently, in order to apply the effective thermal conductivity for microstructures such as a thin film or

nanowire, the macroscopic Fourier's law must be modified based on kinetic theory as follows [27]:

$$\dot{q}_x = -\frac{v}{3}\Lambda \frac{dU}{dT} \frac{dT}{dx} \quad (3)$$

where $\dot{q}_x$ is the net heat flux transported by heat carriers in x-direction, v is the average velocity of the heat carriers, U is the internal energy density per unit volume in J/m³, and dU/dT is the volumetric heat capacity C in J/m³·K. Comparing Eq. (3) with the classical Fourier's law ($\dot{q}_x = -k(dT/dx)$) leads to the thermal conductivity equation as follows [27]:

$$k = \frac{1}{3}Cv\Lambda. \quad (4)$$

By treating C , v , and Λ in the above equation as frequency (ω)-dependent quantities, the thermal conductivity by kinetic theory can be expressed as an integral form to account for the frequency dependence [28]:

$$k = \frac{1}{3} \int C(\omega, T) v(\omega) \Lambda_{eff}(\omega, T) d\omega \quad (5)$$

where Λ_{eff} is the effective mean free path expressed by $\Lambda_{eff}^{-1} = \Lambda_{umkl}^{-1} + \Lambda_{imp}^{-1} + \Lambda_{bdy}^{-1}$ based on Matthiessen's rule. Each mean free path, Λ_{umkl} , Λ_{imp} , and Λ_{bdy} , is caused by phonon-phonon Umklapp scattering, impurity scattering, and boundary scattering, respectively, and can be expressed with frequency (ω), temperature (T), and sample dimension (D) [29,30]:

$$\Lambda_{umkl}^{-1}(\omega, T) = \frac{B_1 \omega^2 T \exp(-B_2/T)}{v_g} \quad \Lambda_{imp}^{-1}(\omega) = \frac{A_1 \omega^4}{v_g} \quad \Lambda_{bdy}^{-1} = D^{-1} \quad (6)$$

where v_g is the group velocity. To account for the frequency dependence, the Born-von Karman dispersion relation ($\omega = \omega_0 \sin(\pi\kappa/2\kappa_D)$) can be used, where $\omega_0 = 2v_s\kappa_D/\pi$ and

$\kappa_D = (6\pi^2 \eta_{PUC})^{1/3}$ for the Debye cutoff wave vector, where v_s is the average sound velocity, and η_{PUC} is the number density of a primitive unit cell in m^{-3} [27,31]. The coefficients A_1 , B_1 , and B_2 in Eq. (6) depend on the material. By integrating Eq. (5) with all parameters described above, more accurate thermal conductivity can be calculated for microscale and nanoscale samples.

To estimate the thermal conductivity of the evaporator and reservoir layer, which consist of single Si wafer, the above approximation can be used. However, because the thickness of evaporator and reservoir layer is around 500 μm , which is the general thickness of a 4-inch Si wafer where the evaporator and reservoir will be fabricated, the thermal conductivity is expected to follow diffusive behavior (i.e., bulk-like). Therefore, thermal conductivity of the evaporator Si layer can be also readily estimated from experimental data of bulk Si. For example, at around 130°C, which is the estimated evaporator's maximum temperature at the initial state of operation, thermal conductivity can be approximated as 105 $\text{W/m}\cdot\text{K}$ from experimental data [32], comparable to 103 $\text{W/m}\cdot\text{K}$ calculated by the kinetic theory with fitting coefficients of $A_1=2.4\text{e-}45 \text{ s}^3$, $B_1=1.7\text{e-}19 \text{ s/K}$, and $B_2=210 \text{ K}$ [31]. For thermal resistance, the active cooling area (i.e., area of evaporator site) was designed as $5\times 5 \text{ mm}^2$, which is large enough size for general MEMS chips. Therefore, the thermal resistance across the Si layer was calculated as 0.19 K/W . Although the thermal conductivity of the Si also depends on the dopant type and doping concentration, which contributes to impurity scattering, doping effects on thermal conductivity are generally limited at around 300 K and below where impurity scattering dominates thermal conductivity because thermal conductivity is significantly dominated by phonon-phonon Umklapp scattering at high temperature [33]. In this study, p-type $\langle 100 \rangle$ 4-inch Si wafer with boron concentration of $1\times 10^{15} \text{ cm}^{-3}$ was used for the fabrication of evaporator and reservoir layer.

2.2.2. Thermal conductivity of wick layer

Because the wick layer is comprised of nanowires and porous Si structure (Fig. 2b), thermal conductivities of both nanowires and porous Si were considered. In the present study, zinc oxide (ZnO) nanowires, which have facile and rapid synthesis method for large-scale applications and good thermal stability, were used to decorate the top surface of the porous Si wick. To calculate the thermal conductivity of ZnO nanowire by the kinetic modeling, the values of fitting parameters (A_1 , B_1 , and B_2) in Eq. (6) were determined by matching the modeling to experimental data for bulk ZnO sample. As a result, the theoretical data with $A_1=8.0\text{e-}44 \text{ s}^3$, $B_1=2.6\text{e-}19 \text{ s/K}$, and $B_2=100 \text{ K}$ showed good agreement with experimental data [34,35] for the bulk sample as shown in Fig. 4. The average sound velocity v_s of 3186 m/s [36] and the number density of a primitive unit cell η_{PUC} of $2.1\text{e}28 \text{ m}^{-3}$ were used for the calculation as ZnO has hexagonal wurtzite structure [37]. Using these parameters, the thermal conductivities of ZnO nanowire for different sample sizes were estimated with respect to the temperature, as seen in Fig. 4. It is noticeable that the significant reduction in thermal conductivity appears as the size of the sample is reduced due to the phonon scattering effects, as expected.

For the microporous Si wick, the matrix phase (Si) and the inclusion phase (air or coolant) can be approximated as a parallel connection (Figs. 2b and 3b), in which the scattering effect is negligible because the pitch (i.e., distance between pore to pore) is not narrow enough to impede the heat flow across the wick structure by the phonon scattering. Therefore, in order to predict the effective thermal conductivity of porous Si wick k_{eff} with the porosity ϕ , a simple effective equation can be explicitly expressed as follows:

$$k_{eff} = (1-\phi)k_m + \phi k_i. \quad (7)$$

Fig. 4. Calculated thermal conductivity of zinc oxide with experimental results for a bulk sample and nanowires of different diameter with respect to temperature.

where k_m and k_i are the thermal conductivity of the matrix phase and of the inclusion phase, respectively. In general, because the inclusion phase in the matrix phase has the low thermal conductivity, the effective thermal conductivity of porous media highly depends on the thermal conductivity of the matrix phase and porosity. For example, if the porous Si wick has a porosity of 0.2, the effective thermal conductivity of the wick is about 0.8 times that of bulk Si layer with same thickness. Because thermal conductivities of each components, participating heat conduction across the proposed cooling device from top of the junction to bottom of the reservoir, were determined through above equations, thermal resistance analysis (Fig. 3b) can be performed to estimate the maximum allowable heat flux of the chip, which can be handled by the proposed cooling device with specifications.

3. Experimental method

3.1. Fabrication of evaporator and reservoir layer

To fabricate the evaporator and reservoir layer with built-in microstructures to extend capillary action at the channel ends, clean p-type <100> 4-inch Si wafer with 10–20 Ω -cm resistivity was etched via a standard photolithography. The fabrication of the reservoir layer was much easier than the evaporator layer was because the reservoir layer contains only a single photolithography step to etch both the reservoir chamber and the liquid channel on the layer. The detail fabrication process of the evaporator and reservoir layer is described and depicted with Fig. S1 in the Supporting Information. Fig. 5 shows the scanning electron microscope (SEM) images of the fabricated evaporator layer. Once the coolant removes the heat by touching the evaporator surface underneath the hot chip, the vapor escapes from the evaporator site through the neck connected to the vapor channels, as seen in Fig. 5a. Fig. 5b shows the zoomed-in view of microstructures at the end of the tapered channels. These microstructures at the entrance of the intermediate chamber will drive the condensed coolant out of the microchannels, spreading liquid across the chamber by distributing the meniscus and extending the capillary action by the

Fig. 5. SEM images of deep reactive-ion etched evaporator layer: (a) neck part where the evaporator site and vapor channels are connected and (b) intermediate chamber, which is the end of the tapered vapor channels where the condensed liquid meniscus overflows by microstructures. Scale bars: 200 μ m for both (a) and (b).

assistance of the microstructures, which achieve rapid refilling of coolant into the reservoir. The channel width at the entrance (Fig. 5a) is 500 μm and gradually decreases until it reaches 100 μm at the end of the channel (Fig. 5b). Because the total length of the channels was 40 mm, the tapered angle of channels was 0.286° .

3.2. Fabrication of wick layer

The vertically aligned microchannels are the crucial feature of the porous wick layer to feed the coolant from the reservoir chamber to the end of pores using capillary pressure before the coolant spreads across the entire wick surface by the decorated nanowires. To fabricate the multiple straight microchannel arrays through the Si substrate, photoelectrochemical etching was used in this study for high-aspect-ratio trenches [38,39]. Once the porous Si wick is fabricated, ZnO nanowires can be synthesized on the wick surface by hydrothermal method at low temperature [24]. The detail fabrication flow of the nanowire-integrated coherent porous Si wick layer is shown in Fig. S2 in the Supporting Information. Fig. 6 shows the SEM images of the nanowire-integrated porous Si wick layer with a porosity of approximately 0.175 and an average pore diameter of 4.5 μm to drive the coolant out of the pore and spread coolant between the entire wick and evaporator surface by the assistance of extended capillary action. After hydrothermal synthesis, the dense nanowire forests were grown on the top surface of the Si wick structure, as seen in Figs. 6a and b. With the assistance of decorated nanowires, the pinned liquid meniscus at the pore ends was broken, and liquid was sucked into the nanochannels generated between individual nanowires. Therefore, the chronic dryout problem in the traditional micro cooling device can be solved by continuous feeding of the coolant from reservoir to evaporator surface.

Fig. 6. SEM images of the nanowire-integrated porous silicon wick layer: (a) top surface view, (b) zoomed-in view of micropore ends decorated by ZnO nanowires, (c) 20° tilted view, and (d) zoomed-in view. Scale bars: (a) 2 μm , (b) 1 μm , (c) 10 μm , and (d) 2 μm .

3.3. Final feature of the device and experimental setup

The final feature of the developed cooling device was fabricated by bonding each of the three layers as shown in Fig. 7. The reservoir chamber was filled with deionized (DI) water at the ambient pressure. Each layer contains tailored design structures to perform desirable functions for continuous feeding of the coolant to remove the heat flux from the chip. The final thickness of the bonded cooling device was less than 2 mm because the three 4-inch Si wafers were stacked. Therefore, this tiny planar feature of the device would be helpful to be utilized in current electronic packages, which are now getting smaller and smaller as MEMS and nanotechnologies are being developed. To test the cooling performance of the fabricated device, qualitative and quantitative experiments were simultaneously performed using a high-speed camera and

Fig. 7. Final device feature of the micromachined cooling device composed of three layers: (a) evaporator layer with microstructures, (b) wick layer with nanowire-decorated coherent porous silicon, and (c) reservoir layer with microstructures. Scale bars: (a) 200 μm , (b) 2 μm , (c) 200 μm , and (d) 5 mm.

thermocouple modules, as seen in Fig. 8. As a heat source, a micro ceramic heater ($5 \times 5 \times 1.75$ mm, MS-M 1000, Sakaguchi E.H Voc Corp, Japan) was mounted on the evaporator site (5×5 mm). The temperature was monitored by a thermocouple wire (L-0044K, Omega Engineering, CT) fixed on the ceramic heater by thermal grease (Thermalcote, Aavid Thermalloy, NH). The current and voltage applied to the heater were kept constant at 0.5 A and 1.6 V, respectively, to provide approximately 130°C , which is the global maximum allowable chip temperature to prevent damages caused by overheating [40-42]. The total heat flux of approximately 32 W/cm^2 was dissipated onto the evaporator site. The high-speed camera was used to observe the movement of two-phase flow in the channel. For the qualitative experiment, the evaporator layer was additionally fabricated on a quartz wafer instead of a Si wafer to verify the two-phase flow

and movement of condensed liquids in the microchannels visually. Using the same recipe of standard photolithography used for the fabrication of the evaporator layer on the 4-inch Si wafer, a hard-baked photoresist mask was patterned on a 4-inch quartz wafer, followed by an anisotropic deep reactive-ion etching (STS-OXIDE MPX APS, SPTS, CA).

Fig. 8. Schematic illustration of the experimental setup to analyze both qualitative and quantitative cooling performance of final micromachined cooling device.

4. Results and discussion

4.1. Continuous feeding of coolant

To demonstrate the wicking ability of the fabricated nanowire-integrated porous Si wick layer, sequential images taken by a high-speed camera were compared to results of the porous Si wick layer without nanowires. Fig. 9a shows the top surface view of the porous Si wick layer where the 5×5 mm porous wick region without nanowires was indicated by an arrow in the figure. For the experiment, the fabricated wick layer was placed on the channel, and the water mixed with 1%

v/v wetting agent (Photo-Flow 200, Kodak, NY) was flowed underneath the layer by a syringe. As a result, the water was unable to overflow at all through the porous wick structure without nanowires even after 5 s because all the liquid menisci were pinned at the end of the pores by the surface tension. However, the nanowire-integrated porous Si wick could push the coolant up out of the pores and spread it across the top surface of the wick due to the enhanced and extended capillary action, as seen in Fig. 9b. The coolant was first sucked into the pores immediately after the coolant touched the bottom of the wick layer and surged up to the pore ends due to the primary capillary pressure. At the pore ends, liquid menisci were able to flow further out of the pore due to the nanowires decorated at the pore ends, resulting in overflowing liquid across the top surface of the wick structure. Therefore, this overflowing liquid kept the entire wick surface wetted and hydrated at all times, overcoming the dryout limitations during device operation.

Fig. 9. Comparison of wicking performance between (a) wick structure without nanowires and (b) nanowire-integrated porous silicon wick structure. Scale bars: 5 mm for both (a) and (b).

4.2. Self-transporting of condensed liquid

Fig. 10 shows the transient movement of both liquid and vapor along the microchannels during the phase-change of coolant (i.e., DI water) with a time interval of 5 s. Once the coolant was evaporated between the evaporator and wick surface, the vapor moved toward the condenser part connected to the copper heat sink. The vapors then returned to the liquid phase where the heat sink was connected. After condensed liquids moved to the intermediate chamber along the tapered microchannel by capillary force, menisci were separated by microstructures and flowed along the sidewalls of the structure, which allowed the liquid to be collected between microstructures, as seen in first three sequential images in Fig. 10. The condensed liquids then

Fig. 10. Transient phase-change of coolant in the evaporator layer and movement of condensed liquid along vapor channels toward the intermediate chamber. The condensed liquids were collected on the microstructures and continued to flow into the liquid channels in the reservoir layer. Time interval: 5 s; scale bar: 5 mm.

dropped down to the liquid channels on the reservoir layer and were transported rapidly into the reservoir chamber, which completed the cooling cycle. Considering the nanowire-integrated porous Si wick structure, the coolant was fed again to the evaporator surface by enhanced capillary force due to the nanowires. Therefore, continuous circulation of the two-phase coolant was successfully achieved during the cooling performance without dryout limitations.

4.3. Cooling performance

For quantitative analysis of cooling performance, the temperature of the heater was continuously monitored using a thermocouple module during the operation of the cooling device. For the experiment, the final feature of the cooling device fabricated on Si substrate (Fig. 7) and DI water were used as a source of testing device and coolant, respectively. Fig. 11 shows the temperature change of the micro ceramic heater, dissipating 32 W/cm^2 heat flux, during cooling operation by the developed device. The initial temperature rapidly dropped to 97°C within 75 sec after the heater was mounted on the evaporator site of the cooler because the heat initially spread through the Si evaporator surface using conduction and was then transferred to liquid coolant underneath the evaporator surface. To demonstrate the significant role of the developed cooling device, the cooler was disassembled from the heater again after 3 min and 40 sec, as seen in Fig. 11. As a result, the heater temperature abruptly increased to the initial temperature, showing that the cooling performance was quantitatively verified by the experiment. Therefore, the developed cooler was able to successfully remove, by means of coolant phase-change, the high heat flux generated by the heater.

Fig. 11. Temperature change of the heat source during cooling by the fabricated passive two-phase cooler. The cooler was removed from the heater after 3 min and 40 sec to verify the cooling performance of the cooler. Heat dissipation: 32 W/cm².

5. Conclusions

In this paper, a passive two-phase micro cooling device was developed to remove heat dissipation from chip-level electronics in which rapid, efficient, and reliable cooling is needed. The main design of the developed cooling device was proposed with three functional layers including evaporator, wick, and reservoir layer to improve and extend capillary actions for continuous circulation of the coolant during the operation. For the evaporator and reservoir layer, a combination of a tapered channel and microstructures was designed to break up the pinned meniscus at the end of the microchannels, providing self-transporting ability of condensed liquid in channels. For the wick layer, a nanowire-integrated microporous Si membrane was developed to overcome the wick dryout problem by driving the coolant out of the pore ends and spreading the coolant on top of the wick surface with the assistance of extended capillary action. The chronic dryout problem in micro cooling devices could be solved by adopting these tailored designs. The microscale heat conduction theory derived from traditional Fourier's law with

classical size effect was used to calculate the effective thermal conductivities of nanowires and porous media in the heat flow direction, which can be effectively used as a basic design tool with the thermal network analysis to determine allowable heat flux. The proposed device was then fabricated by a combination of microfabrication techniques and nanomaterial synthesis. Finally, the wicking and cooling performance of the micromachined cooler were demonstrated both qualitatively and quantitatively with a high-speed camera thermocouple modules, showing that the developed cooler was able to successfully remove the high heat flux dissipated from the heat source using reliable and rapid phase-change process of the coolant. This study shows the feasibility of reliable, continuous, and high-performance micro cooling devices using enhanced capillary forces to address the increasing requirements of thermal management for chip-level electronics.

ASSOCIATED CONTENT

Supporting Information. Detail fabrication flow and process of evaporator, reservoir and wick layer.

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Notes

The authors declare no competing financial interest.

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